Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260M, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECspeed\textsuperscript{2017_fp_base} = 146</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed\textsuperscript{2017_fp_peak} = Not Run</td>
</tr>
</tbody>
</table>

\textbf{CPU2017 License:} 9019  \hspace{2cm} \textbf{Test Date:} Aug-2019
\textbf{Test Sponsor:} Cisco Systems  \hspace{2cm} \textbf{Hardware Availability:} Apr-2019
\textbf{Tested by:} Cisco Systems  \hspace{2cm} \textbf{Software Availability:} May-2019

| Threads | 0 | 30.0 | 60.0 | 90.0 | 120 | 150 | 180 | 210 | 240 | 270 | 300 | 330 | 360 | 390 | 420 | 450 | 480 | 510 | 550 |
|---------|---|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 603.bwaves\_s | 48 |      |      |      |      | 168 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 607.cactuBSSN\_s | 48 |      |      |      |      | 106 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 619.lbm\_s | 48 |      |      |      |      | 124 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 621.wrf\_s | 48 |      |      |      |      | 108 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 627.cam4\_s | 48 |      |      |      |      | 59.0 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 628.pop2\_s | 48 |      |      |      |      | 147 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 638.imagick\_s | 48 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 644.nab\_s | 48 |      |      |      |      |      |     269 |      |      |      |      |      |      |      |      |      |      |      |      |      |
| 649.fotonik3d\_s | 48 |      |      |      |      |      |      |     87.2 |      |      |      |      |      |      |      |      |      |      |      |      |
| 654.roms\_s | 48 |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

\textbf{Hardware}

\textbf{CPU Name:} Intel Xeon Platinum 8260M  
\textbf{Max MHz:} 3900  
\textbf{Nominal:} 2400  
\textbf{Enabled:} 48 cores, 2 chips  
\textbf{Orderable:} 1, 2 chip(s)  
\textbf{Cache L1:} 32 KB I + 32 KB D on chip per core  
\textbf{L2:} 1 MB I+D on chip per core  
\textbf{L3:} 35.75 MB I+D on chip per chip  
\textbf{Other:} None  
\textbf{Memory:} 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
\textbf{Storage:} 1 x 960 GB SATA M.2 SSD  
\textbf{Other:} None

\textbf{Software}

\textbf{OS:} SUSE Linux Enterprise Server 15  
\textbf{Compiler:} C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
\textbf{Parallel:} Yes  
\textbf{Firmware:} Version 4.0.4b released Apr-2019  
\textbf{File System:} xfs  
\textbf{System State:} Run level 3 (multi-user)  
\textbf{Base Pointers:} 64-bit  
\textbf{Peak Pointers:} Not Applicable  
\textbf{Other:} None  
\textbf{Power Management:} --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260M, 2.40GHz)

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>93.1</td>
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<td>169</td>
</tr>
</tbody>
</table>

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc0910f
running on linux-aixk Sat Sep 28 09:09:25 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Platinum 8260M CPU @ 2.40GHz
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 16 17 18 19 20 21 22 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8260M CPU @ 2.40GHz
Stepping: 6
CPU MHz: 2400.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K

(Continued on next page)
**SPEC CPU®2017 Floating Point Speed Result**

**Cisco Systems**
Cisco UCS B200 M5 (Intel Xeon Platinum 8260M, 2.40GHz)  

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
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**Platform Notes (Continued)**

```plaintext
NUMA node0 CPU(s):   0-23  
NUMA node1 CPU(s):   24-47  
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov  
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp  
  lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid  
aperfmpref perf_event_cpufreq, perf_event_socket, perf_event_cpuset, perf_event_tsc, perf_event_jiffies  
tsc_deadline_timer xsave avx f16c rdrcr lahf_lm abm 3dnop prefetch cpuid_fault cpuid  
tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cdqm mpx rdt_a  
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl  
xsavesopt xsaveopt xsaves qm llc cdqm_occup llc cdqm_mtb_total cdqm_mtb_local  
ibpb ibrs ibsr sib dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku  
ospe avx512_vnni arch_capabilities ssbd  
```

/proc/cpuinfo cache data  
  ```plaintext
  cache size : 36608 KB
  ```

From `numactl --hardware`  
WARNING: a numactl 'node' might or might not correspond to a physical chip.  
  ```plaintext
  available: 2 nodes (0-1)  
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23  
  node 0 size: 385615 MB  
  node 0 free: 384790 MB  
  node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47  
  node 1 size: 387015 MB  
  node 1 free: 382726 MB  
  node distances:  
  node 0 1  
  0: 10 21  
  1: 21 10  
```

From `/proc/meminfo`  
  ```plaintext
  MemTotal:      791174136 kB  
  HugePages_Total:       0  
  Hugepagesize:        2048 kB  
```

From `/etc/*release* /etc/*version*`  
`os-release:`  
  ```plaintext
  NAME="SLES"  
  VERSION="15"  
  VERSION_ID="15"  
  PRETTY_NAME="SUSE Linux Enterprise Server 15"  
  ID="sles"  
  ID_LIKE="suse"  
  ANSI_COLOR="0;32"  
  CPE_NAME="cpe:/o:suse:sles:15"  
```

(Continued on next page)
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SPEC CPU®2017 Floating Point Speed Result

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SPECspeed®2017_fp_base = 146
SPECspeed®2017_fp_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

uname -a:
Linux linux-aixk 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 28 06:54

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb6 xfs 45G 16G 30G 35% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

-----------------------------------------------
C | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
-----------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------

C++, C, Fortran | 607.cactuBSSN_s(base)
-----------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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Compiler Version Notes (Continued)

Fortran  |  603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
---------|---------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------------------------------------------------

Fortran, C  |  621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64

(Continued on next page)
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### Base Portability Flags (Continued)

649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

---

### Base Optimization Flags

**C benchmarks:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

**Benchmarks using both Fortran and C:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

**Benchmarks using Fortran, C, and C++:**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

---

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

---

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Tested with SPEC CPU®2017 v1.0.2 on 2019-09-28 12:09:24-0400.
Originally published on 2019-11-04.