SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

**CISCO SYSTEMS**

**Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)**

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<tr>
<td>557.xz_r</td>
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</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Platinum 8256
- **Max MHz:** 3900
- **Nominal:** 3800
- **Enabled:** 8 cores, 2 chips, 2 threads/core
- **Orderable:** 16 Chips
- **L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 16.5 MB I+D on chip per chip
- **L3:** 16.5 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** --
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECLICENSE

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Results Table

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Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/old-cpu2017/lib/intel64:/home/old-cpu2017/lib/ia32:/home/old-cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

SPEC CPU®2017 Integer Rate Result

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems

**Test Date:** Oct-2019
**Hardware Availability:** Apr-2019
**Software Availability:** May-2019

**SPECrate®2017_int_base =**
**SPECrate®2017_int_peak =**

---

**General Notes (Continued)**

Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

**Platform Notes**

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- SNC set to Enabled
- IMC Interleaving set to 1-way Interleave
- Patrol Scrub set to Disabled
- Sysinfo program /home/old-cpu2017/bin/sysinfo
  Rev: 15974 - 2019-05-19 9bcde8f2999c33d61f64985e45859ea9
  running on linux-diml Sat Oct 5 12:00:40 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see:
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
  2 "physical id"s (chips)
  16 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores: 4
  siblings: 8
  physical 0: cores 0 1 5 13
  physical 1: cores 2 5 9 13

(Continued on next page)
**SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.**

Platform Notes (Continued)

From lscpu:
- **Architecture:** x86_64
- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little-Endian
- **CPU(s):** 16
- **On-line CPU(s) list:** 0-15
- **Thread(s) per core:** 2
- **Core(s) per socket:** 4
- **Socket(s):** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
- **Stepping:** 6
- **CPU MHz:** 3800.000
- **CPU max MHz:** 3900.0000
- **CPU min MHz:** 1200.0000
- **BogoMIPS:** 7600.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 16896K
- **NUMA node0 CPU(s):** 0,1,8,9
- **NUMA node1 CPU(s):** 2,3,10,11
- **NUMA node2 CPU(s):** 4,6,12,14
- **NUMA node3 CPU(s):** 5,7,13,15
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pprot mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)

| CPU2017 License: | 9019 |
| Test Sponsor:    | Cisco Systems |
| Tested by:       | Cisco Systems |
| Test Date:       | Oct-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | May-2019 |

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---

**Platform Notes (Continued)**

```
avx512f avx512dq rdseed adx clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaves optxl0 xgetbv xsaveopt xsavec xsave clwb clflushopt clwb intel_pt avx512_vnni
arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 8 9
  node 0 size: 192105 MB
  node 0 free: 190810 MB
  node 1 cpus: 2 3 10 11
  node 1 size: 193529 MB
  node 1 free: 192331 MB
  node 2 cpus: 4 6 12 14
  node 2 size: 193500 MB
  node 2 free: 192346 MB
  node 3 cpus: 5 7 13 15
  node 3 size: 193528 MB
  node 3 free: 192351 MB

  distances:
  node   0   1   2   3
  0:  10  11  21  21
  1:  11  10  21  21
  2:  21  21  10  11
  3:  21  21  11  10

From /proc/meminfo
  MemTotal:       791208168 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
```

(Continued on next page)
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Platform Notes (Continued)

```bash
test run: Oct 4 13:55

Kernel self-reported vulnerability status:
CVE-2017-5754 (Retdwn): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 4 13:55

SPEC is set to: /home/old-cpu2017

```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems  
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)  

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CPU2017 License: 9019  
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### Compiler Version Notes

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<td>C++</td>
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<tr>
<td>Fortran</td>
<td><img src="image" alt="Fortran Notes" /></td>
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### Base Compiler Invocation

- **C benchmarks:**
  - `icc -m64 -std=c11`
- **C++ benchmarks:**
  - `icpc -m64`
- **Fortran benchmarks:**
  - `ifort -m64`
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8256, 3.80GHz)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

The flags files that were used to format this result can be browsed at

You can also download the XML flags source by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

Non-compliant