## Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

<table>
<thead>
<tr>
<th>SPEC CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Oct-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_s</td>
<td>36</td>
<td>7.99</td>
<td>10.4</td>
</tr>
<tr>
<td>gcc_s</td>
<td>36</td>
<td>9.79</td>
<td>10.1</td>
</tr>
<tr>
<td>mcf_s</td>
<td>36</td>
<td>12.6</td>
<td>12.7</td>
</tr>
<tr>
<td>omnetpp_s</td>
<td>36</td>
<td>7.73</td>
<td>7.89</td>
</tr>
<tr>
<td>xalancbmk_s</td>
<td>36</td>
<td>12.4</td>
<td>12.4</td>
</tr>
<tr>
<td>x264_s</td>
<td>36</td>
<td>14.1</td>
<td>14.2</td>
</tr>
<tr>
<td>deepsjeng_s</td>
<td>36</td>
<td>5.48</td>
<td>5.48</td>
</tr>
<tr>
<td>leela_s</td>
<td>36</td>
<td>4.77</td>
<td>4.77</td>
</tr>
<tr>
<td>exchange2_s</td>
<td>36</td>
<td>16.7</td>
<td>16.7</td>
</tr>
<tr>
<td>xz_s</td>
<td>36</td>
<td>23.1</td>
<td>23.2</td>
</tr>
</tbody>
</table>

---

### Hardware

- **CPU Name:** Intel Xeon Gold 6240L
- **Max MHz:** 3900
- **Nominal:** 2600
- **Enabled:** 36 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Orderable:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++, Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

---

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>36</td>
<td>260</td>
<td>6.82</td>
<td>259</td>
<td>6.85</td>
<td>258</td>
<td>6.89</td>
<td>36</td>
<td>222</td>
<td>7.99</td>
<td>221</td>
<td>8.03</td>
<td>223</td>
<td>7.97</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>36</td>
<td>406</td>
<td>9.82</td>
<td>407</td>
<td>9.78</td>
<td>407</td>
<td>9.79</td>
<td>36</td>
<td>395</td>
<td>10.1</td>
<td>396</td>
<td>10.0</td>
<td>395</td>
<td>10.1</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>36</td>
<td>374</td>
<td>12.6</td>
<td>375</td>
<td>12.6</td>
<td>375</td>
<td>12.6</td>
<td>36</td>
<td>372</td>
<td>12.7</td>
<td>371</td>
<td>12.7</td>
<td>374</td>
<td>12.6</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>36</td>
<td>210</td>
<td>7.77</td>
<td>212</td>
<td>7.69</td>
<td>211</td>
<td>7.73</td>
<td>36</td>
<td>206</td>
<td>7.90</td>
<td>207</td>
<td>7.89</td>
<td>212</td>
<td>7.69</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>36</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
<td>12.5</td>
<td>36</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
<td>12.5</td>
<td>114</td>
<td>12.4</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>36</td>
<td>125</td>
<td>14.1</td>
<td>125</td>
<td>14.2</td>
<td>125</td>
<td>14.1</td>
<td>36</td>
<td>125</td>
<td>14.2</td>
<td>124</td>
<td>14.2</td>
<td>125</td>
<td>14.1</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>36</td>
<td>261</td>
<td>5.48</td>
<td>261</td>
<td>5.48</td>
<td>261</td>
<td>5.48</td>
<td>36</td>
<td>261</td>
<td>5.48</td>
<td>261</td>
<td>5.49</td>
<td>261</td>
<td>5.48</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>36</td>
<td>357</td>
<td>4.77</td>
<td>357</td>
<td>4.77</td>
<td>357</td>
<td>4.78</td>
<td>36</td>
<td>358</td>
<td>4.77</td>
<td>357</td>
<td>4.78</td>
<td>358</td>
<td>4.77</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>36</td>
<td>176</td>
<td>16.7</td>
<td>177</td>
<td>16.6</td>
<td>176</td>
<td>16.7</td>
<td>36</td>
<td>176</td>
<td>16.7</td>
<td>176</td>
<td>16.7</td>
<td>176</td>
<td>16.7</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>36</td>
<td>268</td>
<td>23.1</td>
<td>268</td>
<td>23.1</td>
<td>268</td>
<td>23.1</td>
<td>36</td>
<td>266</td>
<td>23.2</td>
<td>266</td>
<td>23.2</td>
<td>266</td>
<td>23.2</td>
</tr>
</tbody>
</table>

---

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

---

**General Notes**

Environment variables set by runcpu before the start of the run:

- `KMP_AFFINITY = "granularity=fine,scatter"
- `LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- `OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


---
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-bo7k Thu Oct 3 15:24:23 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240L CPU @ 2.60GHz
   "physical id"s (chips)
36 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240L CPU @ 2.60GHz
Stepping: 7
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

| SPECspeed®2017_int_base = 10.1 |
| SPECspeed®2017_int_peak = 10.4 |

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

---

**Platform Notes (Continued)**

```plaintext
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bs rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_ppi mba tpr_shadow vni flexpriority ept
vpid fsqgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsavec qsmllc qcm_occup_llc qcm_mbm_total qcm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
   node 0 size: 385604 MB
   node 0 free: 384815 MB
   node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
   node 1 size: 387056 MB
   node 1 free: 386756 MB
   node distances:
   node 0 1
   0: 10 21
   1: 21 10

From /proc/meminfo
MemTotal: 791204696 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
   NAME="SLES"
   VERSION="15"
   VERSION_ID="15"
   PRETTY_NAME="SUSE Linux Enterprise Server 15"
   ID="sles"
   ID_LIKE="suse"

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2019 Standard Performance Evaluation Corporation

Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-bo7k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 3 15:21

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda1 xfs 224G 20G 204G 9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPECSpeed®2017_int_base = 10.1
SPECSpeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 648.exchange2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Optimization Flags (Continued)

C benchmarks (continued):
-LL/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-LL/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-LL/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

602.gcc_s (continued):
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s:\-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s:\-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s:\-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s:\-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s:\-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6240L, 2.60GHz)

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-10-03 05:54:22-0400.
Originally published on 2019-11-04.