**Cisco Systems**

Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>204</td>
<td>204</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>87.3</td>
<td>87.9</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>140</td>
<td>139</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>142</td>
<td>142</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>61.4</td>
<td>61.6</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>202</td>
<td>202</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>89.0</td>
<td>89.5</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>381</td>
<td>381</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>192</td>
<td>192</td>
</tr>
</tbody>
</table>

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-25.28-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** ---

---

**Hardware**

- **CPU Name:** Intel Xeon Gold 6240
- **Max MHz:** 3900
- **Nominal:** 2600
- **Enabled:** 72 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 24.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None
# SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
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<td>880</td>
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<td>874</td>
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<td>870</td>
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<td>204</td>
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<td>203</td>
<td>81.7</td>
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<td>72</td>
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<td>204</td>
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<td>619.lbm_s</td>
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<td>149</td>
<td>60.0</td>
<td><strong>87.3</strong></td>
<td>72</td>
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<tr>
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<td>141</td>
<td>94.2</td>
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<td><strong>139</strong></td>
<td></td>
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<tr>
<td>627.cam4_s</td>
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<td>142</td>
<td><strong>62.6</strong></td>
<td><strong>142</strong></td>
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<td><strong>62.2</strong></td>
<td><strong>142</strong></td>
<td>62.2</td>
<td>142</td>
<td><strong>62.2</strong></td>
<td><strong>143</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
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<td>61.3</td>
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<td>649.fotonik3d_s</td>
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<td>184</td>
<td><strong>83.4</strong></td>
<td><strong>189</strong></td>
<td>82.2</td>
<td>191</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

- `KMP_AFFINITY = "granularity=fine,compact"
- `LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- `OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

### NA:
The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

### Yes:
The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

## Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-75co Fri Oct  4 11:05:22 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
  4 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
Stepping: 5
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECspeed®2017_fp_base = 174
SPECspeed®2017_fp_peak = 174

Cisco Systems
CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)
## Platform Notes (Continued)

```
| L3 cache:        | 25344K |
| NUMA node0 CPU(s): | 0-17   |
| NUMA node1 CPU(s): | 18-35  |
| NUMA node2 CPU(s): | 36-53  |
| NUMA node3 CPU(s): | 54-71  |
| Flags:           | fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pstate ssbd mba ibrs ibpb stibp tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsavec qrm_llc qrm_occup_llc qrm_mbm_total qrm_mbm_local dtherm ida arat pni pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke flush_l1d arch_capabilities
```

```
From /proc/cpuinfo cache data
    cache size : 25344 KB
```

```
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385637 MB
node 0 free: 384623 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387039 MB
node 1 free: 386869 MB
node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
node 2 size: 387068 MB
node 2 free: 379939 MB
node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 3 size: 387066 MB
node 3 free: 386762 MB
node distances:
    node 0 1 2 3
    0: 10 21 21 21
    1: 21 10 21 21
    2: 21 21 10 21
    3: 21 21 21 10
```

```
From /proc/meminfo
    MemTotal: 1583934724 kB
    HugePages_Total: 0
    Hugepagesize: 2048 kB
```

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECspeed®2017_fp_base = 174
SPECspeed®2017_fp_peak = 174

Platform Notes (Continued)

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

  uname -a:
    Linux linux-75co 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB: conditional, IBRS_FW, RSB filling

run-level 3 Oct 4 06:24

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda3 xfs 177G 55G 123G 31% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C480M5.4.0.4g.0.0712190013 07/12/2019
  Memory:
    48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>Compiler</th>
<th>619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base, peak)</th>
</tr>
</thead>
</table>

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECspeed®2017_fp_base = 174
SPECspeed®2017_fp_peak = 174

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
94.roms_s(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
628.pop2_s(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date:  Oct-2019</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byte_recl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECspeed®2017_fp_base = 174
SPECspeed®2017_fp_peak = 174

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs
649.fotonik3d_s: Same as 603.bwaves_s
654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:
621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6240, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Tested with SPEC CPU®2017 v1.0.5 on 2019-10-04 14:05:21-0400.

**SPECspeed®2017_fp_base = 174**
**SPECspeed®2017_fp_peak = 174**

**Peak Optimization Flags (Continued)**

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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