Dell Inc. PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

SPECrater®2017_int_base = 174
SPECrater®2017_int_peak = 180

Hardware
- CPU Name: Intel Xeon Silver 4216
- Max MHz: 3200
- Nominal: 2100
- Enabled: 32 cores, 2 chips, 2 threads/core
- Orderable: 1.2 chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 22 MB I+D on chip per chip
- Other: None
- Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
- Storage: 1 x 960 GB SATA SSD
- Other: None

Software
- OS: SUSE Linux Enterprise Server 15 SP1
  kernel 4.12.14-195-default
- Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux
- Parallel: No
- Firmware: Version 2.3.10 released Aug-2019
- File System: xfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 32/64-bit
- Other: jemalloc memory allocator V5.0.1
- Power Management: None
# SPEC CPU®2017 Integer Rate Result

**Dell Inc.**

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>55</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Dell Inc.</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Dell Inc.</td>
</tr>
</tbody>
</table>

**SPECrater®2017_int_base = 174**

**SPECrater®2017_int_peak = 180**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Rati</th>
<th>Peak</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Rati</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>64</td>
<td>764</td>
<td>133</td>
<td>768</td>
<td>133</td>
<td>64</td>
<td>668</td>
<td>152</td>
<td>665</td>
<td>153</td>
<td>180</td>
<td>180</td>
<td></td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>64</td>
<td>621</td>
<td>146</td>
<td>627</td>
<td>145</td>
<td>64</td>
<td>546</td>
<td>166</td>
<td>547</td>
<td>166</td>
<td>174</td>
<td>174</td>
<td></td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>64</td>
<td>454</td>
<td>228</td>
<td>456</td>
<td>227</td>
<td>64</td>
<td>455</td>
<td>227</td>
<td>454</td>
<td>228</td>
<td>720</td>
<td>720</td>
<td></td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>64</td>
<td>720</td>
<td>117</td>
<td>720</td>
<td>117</td>
<td>64</td>
<td>720</td>
<td>117</td>
<td>719</td>
<td>117</td>
<td>720</td>
<td>720</td>
<td></td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>64</td>
<td>340</td>
<td>199</td>
<td>337</td>
<td>200</td>
<td>64</td>
<td>318</td>
<td>212</td>
<td>318</td>
<td>212</td>
<td>595</td>
<td>595</td>
<td></td>
</tr>
<tr>
<td>525.x264_r</td>
<td>64</td>
<td>334</td>
<td>335</td>
<td>334</td>
<td>335</td>
<td>64</td>
<td>321</td>
<td>350</td>
<td>322</td>
<td>348</td>
<td>720</td>
<td>720</td>
<td></td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>64</td>
<td>515</td>
<td>142</td>
<td>516</td>
<td>142</td>
<td>64</td>
<td>515</td>
<td>142</td>
<td>516</td>
<td>142</td>
<td>516</td>
<td>516</td>
<td></td>
</tr>
<tr>
<td>541.leela_r</td>
<td>64</td>
<td>809</td>
<td>131</td>
<td>804</td>
<td>132</td>
<td>64</td>
<td>809</td>
<td>131</td>
<td>804</td>
<td>132</td>
<td>804</td>
<td>804</td>
<td></td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>64</td>
<td>490</td>
<td>342</td>
<td>489</td>
<td>343</td>
<td>64</td>
<td>490</td>
<td>342</td>
<td>489</td>
<td>343</td>
<td>489</td>
<td>489</td>
<td></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>64</td>
<td>595</td>
<td>116</td>
<td>596</td>
<td>116</td>
<td>64</td>
<td>595</td>
<td>116</td>
<td>596</td>
<td>116</td>
<td>596</td>
<td>596</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECRate®2017_int_base = 174
SPECRate®2017_int_peak = 180

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

General Notes (Continued)

is mitigated in the system as tested and documented.
Benchmark run from a 120 GB ramdisk created with the cmd:
"mount -t tmpfs -o size=120G tmpfs /mnt/ramdisk".
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS settings:
ADDDC setting disabled
Sub NUMA Cluster enabled
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor enabled
CPU Interconnect Bus Link Power Management enabled
PCI ASPM L1 Link Power Management enabled

Sysinfo program /mnt/ramdisk/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbe6e46a485a0011
running on linux-g3o8 Sat Oct 26 13:36:21 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32

(Continued on next page)
### SPEC CPU®2017 Integer Rate Result

**Dell Inc.**

**PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>174</td>
<td>180</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License</td>
<td>55</td>
</tr>
<tr>
<td>Test Sponsor</td>
<td>Dell Inc.</td>
</tr>
<tr>
<td>Tested by</td>
<td>Dell Inc.</td>
</tr>
<tr>
<td>Test Date</td>
<td>Oct-2019</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Jun-2019</td>
</tr>
</tbody>
</table>

#### Platform Notes (Continued)

```
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From `lscpu`:
- **Architecture**: x86_64
- **CPU op-mode(s)**: 32-bit, 64-bit
- **Byte Order**: Little Endian
- **Address sizes**: 46 bits physical, 48 bits virtual
- **CPU(s)**: 64
- **On-line CPU(s) list**: 0-63
- **Thread(s) per core**: 2
- **Core(s) per socket**: 16
- **Socket(s)**: 2
- **NUMA node**: 4
- **Vendor ID**: GenuineIntel
- **CPU family**: 6
- **Model**: 85
- **Model name**: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
- **Stepping**: 6
- **CPU MHz**: 2100.000
- **BogoMIPS**: 4200.00
- **Virtualization**: VT-x
- **L1d cache**: 32K
- **L1i cache**: 32K
- **L2 cache**: 1024K
- **L3 cache**: 22528K
- **NUMA node0 CPU(s)**: 0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60
- **NUMA node1 CPU(s)**: 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61
- **NUMA node2 CPU(s)**: 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
- **NUMA node3 CPU(s)**: 3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63
- **Flags**: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pni ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cmpx mingle rdtscp rdvi rdseed adx smap clflushopt clwb intel_pt avx512sd avx512vw avx512vl xsaveopt xsaves xsavec xatment xsaves cqm_llc cqm_occupa_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld arch_capabilities

```
/proc/cpuinfo cache data
cache size : 22528 KB
```

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a

(Continued on next page)
Dell Inc.  
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

**SPEC CPU®2017 Integer Rate Result**  
Copyright 2017-2019 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 174  
SPECrate®2017_int_peak = 180

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Test Date:** Oct-2019  
**Tested by:** Dell Inc.  
**Hardware Availability:** Aug-2019  
**Software Availability:** Jun-2019  

**Platform Notes (Continued)**

```
physical chip.  
   available: 4 nodes (0-3)  
node 0 cpus:  0  4  8 12 16 20 24 28 32 36 40 44 48 52 56 60  
node 0 size: 95117 MB  
node 0 free: 90083 MB  
node 1 cpus:  1  5  9 13 17 21 25 29 33 37 41 45 49 53 57 61  
node 1 size: 96764 MB  
node 1 free: 96609 MB  
node 2 cpus:  2  6 10 14 18 22 26 30 34 38 42 46 50 54 58 62  
node 2 size: 96764 MB  
node 2 free: 96584 MB  
node 3 cpus:  3  7 11 15 19 23 27 31 35 39 43 47 51 55 59 63  
node 3 size: 96763 MB  
node 3 free: 96594 MB  
node distances:  
     node 0  1  2  3  
     0: 10 21 11 21  
     1: 21 10 21 11  
     2: 11 21 10 21  
     3: 21 11 21 10  

From /proc/meminfo  
   MemTotal:        394660960 kB  
   HugePages_Total:       0  
   Hugepagesize:        2048 kB  

From /etc/*release* /etc/*version*  
   os-release:  
      NAME="SLES"  
      VERSION="15-SP1"  
      VERSION_ID="15.1"  
      PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"  
      ID="sles"  
      ID_LIKE="suse"  
      ANSI_COLOR="0;32"  
      CPE_NAME="cpe:/o:suse:sles:15:sp1"  

uname -a:  
   Linux linux-g3ob 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)  
   x86_64 x86_64 x86_64 GNU/Linux  

Kernel self-reported vulnerability status:  
   CVE-2018-3620 (L1 Terminal Fault): Not affected  
   Microarchitectural Data Sampling: Not affected  
   CVE-2017-5754 (Meltdown): Not affected  
   CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
```

(Continued on next page)
### Dell Inc.

**PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>174</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>180</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Test Date:** Oct-2019  
**Hardware Availability:** Aug-2019  
**Tested by:** Dell Inc.  
**Software Availability:** Jun-2019

#### Platform Notes (Continued)

- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
- CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

```bash
rpm -q spec
```

---

**Compiler Version Notes**

```
C | 502.gcc_r(peak)
```

---

Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

```
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base, peak)
```

---

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

(Continued on next page)
Compiler Version Notes (Continued)

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
                     | 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++     | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
                     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++     | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
                     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
(Continued on next page)
### Compiler Version Notes (Continued)

Intel (R) C++ Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

Fortran | 548.exchange2_r(base, peak)
---

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

### Base Compiler Invocation

**C benchmarks:**

```
icc -m64 -std=c11
```

**C++ benchmarks:**

```
icpc -m64
```

**Fortran benchmarks:**

```
ifort -m64
```

### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

```
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
```

(Continued on next page)
SPEC CPU®2017 Integer Rate Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrate®2017_int_base = 174
SPECrate®2017_int_peak = 180

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

Base Optimization Flags (Continued)

C benchmarks (continued):
- -qopt-mem-layout-trans=4
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- -lqkmalloc

C++ benchmarks:
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- -lqkmalloc

Fortran benchmarks:
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- -lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64

(Continued on next page)
Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPEC CPU®2017 Integer Rate Result

SPECrate®2017_int_base = 174
SPECrate®2017_int_peak = 180

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

Peak Portability Flags (Continued)

541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: basepeak = yes

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: basepeak = yes

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrate®2017_int_base = 174
SPECrate®2017_int_peak = 180

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

Peak Optimization Flags (Continued)

541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-10-26 14:36:21-0400.
Originally published on 2019-11-12.