## Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>166</td>
<td>177</td>
</tr>
</tbody>
</table>

---

### Hardware

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Silver 4216</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz:</td>
<td>3200</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2100</td>
</tr>
<tr>
<td>Enabled:</td>
<td>32 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>22 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>384 GB (12 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 960 GB SATA SSD</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 SP1 kernel 4.12.14-195-default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 2.3.10 released Aug-2019</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
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<tr>
<td>Power Management:</td>
<td>None</td>
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## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>64</td>
<td>1513</td>
<td>424</td>
<td>1513</td>
<td>424</td>
<td>32</td>
<td>741</td>
<td>433</td>
<td></td>
<td>740</td>
<td>433</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>64</td>
<td>595</td>
<td>136</td>
<td>593</td>
<td>137</td>
<td>64</td>
<td>593</td>
<td>137</td>
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<td>593</td>
<td>137</td>
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<tr>
<td>508.namd_r</td>
<td>64</td>
<td>509</td>
<td>119</td>
<td>513</td>
<td>118</td>
<td>64</td>
<td>505</td>
<td>120</td>
<td></td>
<td>502</td>
<td>121</td>
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<tr>
<td>510.parest_r</td>
<td>64</td>
<td>1708</td>
<td>98.0</td>
<td>1702</td>
<td>98.3</td>
<td>32</td>
<td>703</td>
<td>119</td>
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<td>702</td>
<td>119</td>
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<tr>
<td>511.povray_r</td>
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<td>816</td>
<td>183</td>
<td>819</td>
<td>182</td>
<td>64</td>
<td>685</td>
<td>218</td>
<td>686</td>
<td>218</td>
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<td>519.lbm_r</td>
<td>64</td>
<td>699</td>
<td>96.5</td>
<td>699</td>
<td>96.5</td>
<td>32</td>
<td>670</td>
<td>101</td>
<td>670</td>
<td>101</td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>64</td>
<td>815</td>
<td>176</td>
<td>819</td>
<td>175</td>
<td>32</td>
<td>377</td>
<td>190</td>
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<tr>
<td>526.blender_r</td>
<td>64</td>
<td>542</td>
<td>180</td>
<td>541</td>
<td>180</td>
<td>64</td>
<td>540</td>
<td>181</td>
<td>540</td>
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<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>64</td>
<td>615</td>
<td>182</td>
<td>616</td>
<td>182</td>
<td>64</td>
<td>594</td>
<td>188</td>
<td>602</td>
<td>186</td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>64</td>
<td>424</td>
<td>376</td>
<td>420</td>
<td>379</td>
<td>64</td>
<td>420</td>
<td>379</td>
<td>421</td>
<td>378</td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>64</td>
<td>391</td>
<td>276</td>
<td>393</td>
<td>274</td>
<td>391</td>
<td>274</td>
<td>391</td>
<td>274</td>
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<td></td>
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<tr>
<td>549.fotonik3d_r</td>
<td>64</td>
<td>1839</td>
<td>136</td>
<td>1845</td>
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<td>1837</td>
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<tr>
<td>554.roms_r</td>
<td>64</td>
<td>1300</td>
<td>78.2</td>
<td>1306</td>
<td>77.9</td>
<td>32</td>
<td>523</td>
<td>97.2</td>
<td>520</td>
<td>97.8</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/mnt/ramdisk/cpu2017/lib/intel64"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

(Continued on next page)
General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Benchmark run from a 120 GB ramdisk created with the cmd:
"mount -t tmpfs -o size=120G tmpfs /mnt/ramdisk".
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

Platform Notes

BIOS settings:
ADDDC setting disabled
Sub NUMA Cluster enabled
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor enabled
PCI ASPM L1 Link Power Management enabled

Sysinfo program /mnt/ramdisk/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on linux-g3ob Sat Oct 26 20:08:34 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrater®2017_fp_base = 166
SPECrater®2017_fp_peak = 177

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrate (Continued)

Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrater®2017_fp_base = 166
SPECrater®2017_fp_peak = 177

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Platform Notes (Continued)

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 64
On-line CPU(s) list: 0–63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60
NUMA node1 CPU(s): 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61
NUMA node2 CPU(s): 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
NUMA node3 CPU(s): 3, 7, 11, 15, 19, 23, 27, 31, 35, 39, 43, 47, 51, 55, 59, 63
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pppin ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 iplei invpcid rtm cmx mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsxopt xsaves cqm_lcc qm_occup_lcc qm_mbb_total qm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0–3)

(Continued on next page)
Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

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Platform Notes (Continued)

node 0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60
node 0 size: 95117 MB
node 0 free: 90031 MB
node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61
node 1 size: 96764 MB
node 1 free: 96562 MB
node 2 cpus: 2 6 10 14 18 22 26 30 34 38 42 46 50 54 58 62
node 2 size: 96764 MB
node 2 free: 96542 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63
node 3 size: 96763 MB
node 3 free: 96547 MB
node distances:
node 0 1 2 3
0: 10 21 11 21
1: 21 10 21 11
2: 11 21 10 21
3: 21 11 21 10

From /proc/meminfo
MemTotal: 394660960 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-g3ob 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization

(Continued on next page)
Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrate®2017_fp_base = 166
SPECrate®2017_fp_peak = 177

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

Platform Notes (Continued)

CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Oct 26 08:25 last=5

SPECr is set to: /mnt/ramdisk/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
tmpfs tmpfs 120G 4.5G 116G 4% /mnt/ramdisk

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.3.10 08/15/2019
Vendor: Dell Inc.
Product: PowerEdge R440
Product Family: PowerEdge
Serial: B5XZZL2

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x 00AD00B300AD HMA84GR7AFR4N-VK 32 GB 2 rank 2666
4x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
| 544.nab_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrater®2017_fp_base = 166
SPECrater®2017_fp_peak = 177

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

Compiler Version Notes (Continued)

C++, C  | 511.povray_r(base, peak) 526.blender_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------

C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------

Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------

Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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-----------------------------------------------------

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019
Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

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SPECrate®2017_fp_peak = 177

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Oct-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Jun-2019</td>
</tr>
</tbody>
</table>

### Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

### Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
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<tbody>
<tr>
<td>503.bwaves_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX -funsigned-char</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

### Base Optimization Flags

C benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only

(Continued on next page)
Dell Inc.
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

| SPECrate\textsuperscript{2017\_fp\_base} = 166 |
| SPECrate\textsuperscript{2017\_fp\_peak} = 177 |

| CPU\textsuperscript{2017 License} | 55 |
| Test Sponsor | Dell Inc. |
| Tested by | Dell Inc. |

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

Base Optimization Flags (Continued)

C++ benchmarks (continued):
-\texttt{-qopt-mem-layout-trans=4}

Fortran benchmarks:
-\texttt{-xCORE-AVX2 \ -ipo \ -O3 \ -no-prec-div \ -qopt-prefetch \ -ffinite-math-only}
-\texttt{-qopt-mem-layout-trans=4 \ -auto \ -nostandard-realloc-lhs}
-\texttt{-align array32byte}

Benchmarks using both Fortran and C:
-\texttt{-xCORE-AVX2 \ -ipo \ -O3 \ -no-prec-div \ -qopt-prefetch \ -ffinite-math-only}
-\texttt{-qopt-mem-layout-trans=4 \ -auto \ -nostandard-realloc-lhs}
-\texttt{-align array32byte}

Benchmarks using both C and C++:
-\texttt{-xCORE-AVX2 \ -ipo \ -O3 \ -no-prec-div \ -qopt-prefetch \ -ffinite-math-only}
-\texttt{-qopt-mem-layout-trans=4 \ -auto \ -nostandard-realloc-lhs}
-\texttt{-align array32byte}

Peak Compiler Invocation

C benchmarks:
\texttt{icc \ -m64 \ -std=c11}

C++ benchmarks:
\texttt{icpc \ -m64}

Fortran benchmarks:
\texttt{ifort \ -m64}

Benchmarks using both Fortran and C:
\texttt{ifort \ -m64 \ icc \ -m64 \ -std=c11}

Benchmarks using both C and C++:
\texttt{icpc \ -m64 \ icc \ -m64 \ -std=c11}

Benchmarks using Fortran, C, and C++:
\texttt{icpc \ -m64 \ icc \ -m64 \ -std=c11 \ ifort \ -m64}
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECrate®2017_fp_base = 166
SPECrate®2017_fp_peak = 177

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Oct-2019
Hardware Availability: Aug-2019
Software Availability: Jun-2019

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.ibm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

(Continued on next page)
Dell Inc. PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

<table>
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<tr>
<th>SPECrate®2017_fp_base</th>
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**SPEC CPU 2017 Licensing**

- **CPU2017 License:** 55
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### Peak Optimization Flags (Continued)

Benchmarks using both C and C++:

- `511.povray_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
- 526.blender_r -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:

- `xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.