Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 259</th>
<th>SPECrate®2017_fp_peak = 263</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
<td>Test Date: Oct-2019</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

**Hardware**
- **CPU Name:** Intel Xeon Platinum 8276L
- **Max MHz:** 4000
- **Nominal:** 2200
- **Enabled:** 56 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 38.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 600 GB 15K RPM SAS HDD
- **Other:** None

**Software**
- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** default
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>288</td>
<td>227</td>
<td>385</td>
<td>678</td>
<td>385</td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
```
sync; echo 3> /proc/sys/vm/drop_caches
```

(Continued on next page)
Cisco Systems
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SPECrate®2017_fp_base = 259
SPECrate®2017_fp_peak = 263

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb1e6e46a485a0011
running on linux-ylla Fri Oct 25 05:33:48 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz
2 "physical id"s (chips)
112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per core: 28

(Continued on next page)
Cisco Systems  
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)  

**SPEC CPU®2017 Floating Point Rate Result**

| SPECrate®2017_fp_base = 259 |
| SPECrate®2017_fp_peak = 263 |

- **CPU2017 License:** 9019  
- **Test Sponsor:** Cisco Systems  
- **Tested by:** Cisco Systems  
- **Test Date:** Oct-2019  
- **Hardware Availability:** Apr-2019  
- **Software Availability:** May-2019  

### Platform Notes (Continued)

- **Socket(s):** 2  
- **NUMA node(s):** 4  
- **Vendor ID:** GenuineIntel  
- **CPU family:** 6  
- **Model:** 85  
- **Model name:** Intel(R) Xeon(R) Platinum 8276L CPU @ 2.20GHz  
- **Stepping:** 7  
- **CPU MHz:** 2200.000  
- **CPU max MHz:** 4000.000  
- **CPU min MHz:** 1000.000  
- **BogoMIPS:** 4400.00  
- **Virtualization:** VT-x  
- **L1d cache:** 32K  
- **L1i cache:** 32K  
- **L2 cache:** 1024K  
- **L3 cache:** 39424K  

NUMA node0 CPU(s): 0-3, 7, 14-17, 21-23, 56-59, 63-65, 70-73, 77-79  
NUMA node1 CPU(s): 4-6, 10-13, 18-20, 24-27, 60-62, 66-69, 74-76, 80-83  
NUMA node2 CPU(s): 28-31, 35-37, 42-45, 49-51, 84-87, 91-93, 98-101, 105-107  
NUMA node3 CPU(s): 32-34, 38-41, 46-48, 52-55, 88-90, 94-97, 102-104, 108-111  

**Flags:**  
- fpu vme de pse tsc msr pae mce cx8 apic sep mpe mmx cmov  
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp  
- lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid  
- aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3  
- sdbg fxsr sse2 ssse sse3 sbd gxm cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt  
- tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault  
- epb cat_l3 cpd_l3 invpcid_single intel_pinn tpr_shadow vmx flexpriority ept  
- vpid fsbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmx mpx rdt_a  
- avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl  
- xsaveopt xsave xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local  
- ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pkp  
- ospke avx512_vnni arch_capabilities ssbd  

/proc/cpuinfo cache data  
- cache size: 39424 KB  

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.  
- available: 4 nodes (0-3)  
  - node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 24 25 56 57 58 59 63 64 65 70 71 72 73 77 78 79  
  - node 0 size: 192072 MB  
  - node 0 free: 177080 MB  
  - node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81  
  - node 1 size: 193525 MB  
  - node 1 free: 182039 MB

(Continued on next page)
**Cisco Systems**
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---

**Platform Notes (Continued)**

```
node 2 cpus: 28 29 30 31 35 36 37 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100
                              101 105 106 107
node 2 size: 193525 MB
node 2 free: 181958 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 88 89 90 94 95 96 97 102 103 104
                              108 109 110 111
node 3 size: 193522 MB
node 3 free: 182045 MB
node distances:
node 0  1  2  3                      
0: 10 11 21 21                      
1: 11 10 21 21                      
2: 21 21 10 11                      
3: 21 21 11 10
```

From /proc/meminfo

```
MemTotal:       791189884 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From /etc/*release* /etc/*version*

```
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

uname -a:

```bash
Linux linux-ylla 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault)**: No status reported
- **Microarchitectural Data Sampling**: No status reported
- **CVE-2017-5754 (Meltdown)**: Not affected
- **CVE-2018-3639 (Speculative Store Bypass)**: Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1)**: Mitigation: __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2)**: Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

```
run-level 3 Oct 24 20:08
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECraten®2017_fp_base = 259
SPECraten®2017_fp_peak = 263

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 xfs 559G 115G 445G 21% /

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP22380ZAS

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak) |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
==============================================================================

==============================================================================
| C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak) |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| (Continued on next page) |
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roms_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

(Continued on next page)
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CPU2017 License: 9019
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Tested by: Cisco Systems

Test Date: Oct-2019
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Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r -DSPEC_LP64
507.cactuBSSN_r -DSPEC_LP64
508.namd_r -DSPEC_LP64
510.parest_r -DSPEC_LP64
511.povray_r -DSPEC_LP64
519.ibm_r -DSPEC_LP64
521.wrf_r -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r -DSPEC_LP64
544.nab_r -DSPEC_LP64
549.fotonik3d_r -DSPEC_LP64
554.roms_r -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

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SPECratenfp_base = 259
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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECrate®2017_fp_base = 259
SPECrate®2017_fp_peak = 263

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8276L, 2.20GHz)

SPECrate®2017_fp_base = 259
SPECrate®2017_fp_peak = 263

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Tested with SPEC CPU®2017 v1.1.0 on 2019-10-25 08:33:47-0400.
Originaly published on 2019-11-25.

Peak Optimization Flags (Continued)

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.