Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6230N, 2.30GHz)

**SPEC CPU®2017** Integer Rate Result

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Test Date:** Oct-2019

**Tested by:** Cisco Systems

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

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### Copies

| [ ] | 0  | 20  | 40  | 60  | 80  | 100 | 120 | 140 | 160 | 180 | 200 | 220 | 240 | 260 | 280 | 300 | 320 | 340 | 360 | 380 | 400 | 420 | 440 | 460 | 480 |
|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 500.perlbench_r | 80 | 173 |
| 502.gcc_r | 80 | 185 |
| 505.mcf_r | 80 | 205 |
| 520.omnetpp_r | 80 | 151 |
| 523.xalancbmk_r | 80 | 251 |
| 525.x264_r | 80 | 463 |
| 531.deepsjeng_r | 80 | 189 |
| 541.leela_r | 80 | 177 |
| 548.exchange2_r | 80 | 461 |
| 557.xz_r | 80 | 150 |

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### Hardware

**CPU Name:** Intel Xeon Gold 6230N

**Max MHz:** 3900

**Nominal:** 2300

Enabled: 40 cores, 2 chips, 2 threads/core

Orderable: 1.2 Chips

Cache L1: 32 KB I + 32 KB D on chip per core

L2: 1 MB I+D on chip per core

L3: 27.5 MB I+D on chip per chip

Other: None

Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)

Storage: 1 x 240 GB M.2 SATA SSD

Other: None

---

### Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default

**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;

Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux

**Parallel:** No

**Firmware:** Version 4.0.4g released Jul-2019

**File System:** btrfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** Not Applicable

**Other:** None

**Power Management:** default

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**SPECrate®2017_int_base =** 228

**SPECrate®2017_int_peak =** Not Run
Spectramark analyses of Cisco Systems Cisco UCS C220 M5 (Intel Xeon Gold 6230N, 2.30GHz) SPEC CPU®2017 Integer Rate Result

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SPECrater®2017_int_base = 228
SPECrater®2017_int_peak = Not Run

CPU2017 License: 9019
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Results Table

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<td>150</td>
<td>574</td>
<td>150</td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

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Cisco UCS C220 M5 (Intel Xeon Gold 6230N, 2.30GHz)  

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**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

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## General Notes (Continued)

```bash
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

## Platform Notes

**BIOS Settings:**  
Intel HyperThreading Technology set to Enabled  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled

Sysinfo program: `/home/cpu2017/bin/sysinfo`  
Rev: r6365 of 2019-08-21 295195f888a3d7ed81e646a485a0011  
running on linux-cud8 Mon Oct 21 22:20:12 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From `/proc/cpuinfo`

```
model name : Intel(R) Xeon(R) Gold 6230N CPU @ 2.30GHz
  2 "physical id"s (chips)
    80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
   cpu cores : 20
   siblings : 40
   physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
   physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
```

From `lscpu`:

```
Architecture:      x86_64
CPU op-mode(s):   32-bit, 64-bit
Byte Order:       Little Endian
CPU(s):           80
On-line CPU(s) list: 0-79
Thread(s) per core:  2
Core(s) per socket:  20
Socket(s):        2
NUMA node(s):     4
Vendor ID:        GenuineIntel
```

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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230N, 2.30GHz)

CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Gold 6230N CPU @ 2.30GHz
Stepping:            7
CPU MHz:             2300.000
CPU max MHz:         3500.0000
CPU min MHz:         1000.0000
BogoMIPS:            4600.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            28160K
NUMA node0 CPU(s):   0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s):   3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s):   20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s):   23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtstes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtr pr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat l3 cdp l3 invpcid_single intel_ppin mba tpr_shadow vmmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 emms invpcid rtm cmp mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xsavec xsaves cqm_l1c cqm_occurence cqm_mbm_individual_cqm_mbm_total
cqm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req
kpu ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
nodes 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 192103 MB
node 0 free: 191720 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 193497 MB
node 1 free: 193146 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 193526 MB
node 2 free: 193221 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 193525 MB

(Continued on next page)
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Platform Notes (Continued)

node 3 free: 193302 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791197064 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 21 20:03

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 224G 38G 186G 17% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019

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Tested by: Cisco Systems

Platform Notes (Continued)

Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C
| 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) |
| 525.x264_r(base) 557.xz_r(base) |

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
| 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) |
| 541.leela_r(base) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran
| 548.exchange2_r(base) |

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

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**Base Compiler Invocation (Continued)**

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

**Base Portability Flags**

```bash
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

**Base Optimization Flags**

C benchmarks:
```bash
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

C++ benchmarks:
```bash
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:
```bash
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230N, 2.30GHz) | SPECrate\textsuperscript{\textregistered}2017\_int\_base = 228
| SPECrate\textsuperscript{\textregistered}2017\_int\_peak = Not Run

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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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