## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Gold 6252N, 2.30GHz)  

**SPECraten®2017 int_base = 273**  
**SPECraten®2017 int_peak = Not Run**

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Cisco Systems</th>
<th>Hardware Availability:</th>
<th>Oct-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
<tr>
<td>CPU2017 License:</td>
<td>9019</td>
<td>Test Date:</td>
<td></td>
</tr>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Gold 6252N</td>
<td>Max MHz:</td>
<td>3600</td>
</tr>
<tr>
<td>Max MHz:</td>
<td>3600</td>
<td>Nominal:</td>
<td>2300</td>
</tr>
<tr>
<td>Enabled:</td>
<td>48 cores, 2 chips, 2 threads/core</td>
<td>Orderable:</td>
<td>1,2 Chips</td>
</tr>
<tr>
<td>Orderable:</td>
<td></td>
<td>Cache L1:</td>
<td>32 KB I+32 KB D on chip per core</td>
</tr>
<tr>
<td>Cache L1:</td>
<td></td>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td></td>
<td>L3:</td>
<td>35.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
<td>Storage:</td>
<td>1 x 600 GB 15K RPM SAS HDD</td>
</tr>
<tr>
<td>Software:</td>
<td></td>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64)</td>
</tr>
<tr>
<td>Compiler:</td>
<td></td>
<td>4.12.14-23-default</td>
<td></td>
</tr>
<tr>
<td>Fortran:</td>
<td></td>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;</td>
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<tr>
<td>Parallel:</td>
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<td>Fortran:</td>
<td>Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Firmware:</td>
<td></td>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td></td>
<td>Base Pointers:</td>
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</tr>
<tr>
<td>Base Pointers:</td>
<td></td>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other:</td>
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<td>Other:</td>
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<td>Power Management:</td>
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### Copies

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>96</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>96</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>96</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>96</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>96</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>96</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>96</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>96</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>96</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base (273)**
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6252N, 2.30GHz) SPECrati

SPECrati®2017_int_base = 273
SPECrati®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</thead>
<tbody>
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<tr>
<td>520.omnetpp_r</td>
<td>96</td>
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<td>714</td>
<td>177</td>
<td>715</td>
<td>176</td>
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<td>523.xalancbmk_r</td>
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<td>344</td>
<td>295</td>
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<tr>
<td>525.x264_r</td>
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<td>557</td>
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<td>558</td>
<td>301</td>
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<tr>
<td>531.deepsjeng_r</td>
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<td>226</td>
<td>487</td>
<td>226</td>
<td>487</td>
<td>226</td>
</tr>
<tr>
<td>541.leela_r</td>
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<td>218</td>
<td>731</td>
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<tr>
<td>548.exchange2_r</td>
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<td>556</td>
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<td>553</td>
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<td>557.xz_r</td>
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<td>182</td>
<td>570</td>
<td>182</td>
<td>572</td>
<td>181</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6252N, 2.30GHz)

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SPECrate®2017

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ebdl6e46a485a0011
running on linux-ylla Mon Oct 21 23:25:11 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel

(Continued on next page)
Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6252N, 2.30GHz)

SPECrater²017_int_base = 273
SPECrater²017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

---

Platform Notes (Continued)

CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6252N CPU @ 2.30GHz
Stepping: 7
CPU MHz: 2300.000
CPU max MHz: 3600.0000
CPU min MHz: 1000.0000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,19,20,48-51,55-57,61-63,67,68
NUMA node1 CPU(s): 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
NUMA node2 CPU(s): 24-27,31-33,37-39,43,44,72-75,79-81,85-87,91,92
NUMA node3 CPU(s): 28-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebpx cat_13 cpd_13 invpcid_single intel_pinn mba tpr_shadow vmni flexpriority ept vpid fsgrbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsave vmmarch xgetbv1 xsaves cqm_llc cqm_occu_all cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pkp ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68
node 0 size: 192102 MB
node 0 free: 191750 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71
node 1 size: 193526 MB
node 1 free: 193095 MB
node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92
node 2 size: 193526 MB
node 2 free: 193216 MB
node 3 cpus: 28 29 30 34 35 36 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95
node 3 size: 193494 MB

(Continued on next page)
## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6252N, 2.30GHz)

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<td>May-2019</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

node 3 free: 193278 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791192964 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-ylla 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 21 19:26

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 xfs 559G 70G 490G 13% /

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6252N, 2.30GHz)

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Platform Notes (Continued)

Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP22380ZAS

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
| 525.x264_r(base) 557.xz_r(base)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
| 541.leela_r(base)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 548.exchange2_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

(Continued on next page)
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Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc
Cisco Systems

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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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