Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Specification</th>
<th>Specrate®2017_int_base</th>
<th>Specrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>2017 Integer Rate Result</td>
<td>204</td>
<td>213</td>
</tr>
</tbody>
</table>

Hardware

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Gold 5220</td>
</tr>
<tr>
<td>Max MHz:</td>
<td>3900</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2200</td>
</tr>
<tr>
<td>Enabled:</td>
<td>36 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>24.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 240 GB M.2 SATA SSD</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

Software

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.4g released Jul-2019</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management:</td>
<td>default</td>
</tr>
</tbody>
</table>

Copies

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>72</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>72</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>72</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>72</td>
</tr>
</tbody>
</table>

Specrate®2017_int_base (204) Specrate®2017_int_peak (213)
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>72</td>
<td>738</td>
<td>155</td>
<td>737</td>
<td>155</td>
<td>735</td>
<td>156</td>
<td>72</td>
<td>641</td>
<td>179</td>
<td>641</td>
<td>179</td>
<td>641</td>
<td>179</td>
<td>641</td>
<td>179</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>72</td>
<td>605</td>
<td>168</td>
<td>604</td>
<td>169</td>
<td>601</td>
<td>170</td>
<td>72</td>
<td>530</td>
<td>192</td>
<td>530</td>
<td>192</td>
<td>532</td>
<td>192</td>
<td>532</td>
<td>192</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>72</td>
<td>431</td>
<td>270</td>
<td>431</td>
<td>270</td>
<td>431</td>
<td>270</td>
<td>72</td>
<td>430</td>
<td>271</td>
<td>433</td>
<td>269</td>
<td>432</td>
<td>270</td>
<td>432</td>
<td>270</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>72</td>
<td>675</td>
<td>140</td>
<td>676</td>
<td>140</td>
<td>677</td>
<td>140</td>
<td>72</td>
<td>675</td>
<td>140</td>
<td>677</td>
<td>140</td>
<td>678</td>
<td>139</td>
<td>678</td>
<td>139</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>72</td>
<td>333</td>
<td>228</td>
<td>333</td>
<td>228</td>
<td>333</td>
<td>228</td>
<td>72</td>
<td>307</td>
<td>248</td>
<td>307</td>
<td>248</td>
<td>307</td>
<td>248</td>
<td>307</td>
<td>248</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>72</td>
<td>310</td>
<td>406</td>
<td>310</td>
<td>406</td>
<td>310</td>
<td>406</td>
<td>72</td>
<td>298</td>
<td>423</td>
<td>298</td>
<td>423</td>
<td>298</td>
<td>423</td>
<td>298</td>
<td>423</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>72</td>
<td>497</td>
<td>166</td>
<td>497</td>
<td>166</td>
<td>497</td>
<td>166</td>
<td>72</td>
<td>497</td>
<td>166</td>
<td>497</td>
<td>166</td>
<td>497</td>
<td>166</td>
<td>497</td>
<td>166</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>72</td>
<td>779</td>
<td>153</td>
<td>771</td>
<td>155</td>
<td>780</td>
<td>153</td>
<td>72</td>
<td>770</td>
<td>155</td>
<td>771</td>
<td>155</td>
<td>780</td>
<td>153</td>
<td>780</td>
<td>153</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>72</td>
<td>474</td>
<td>398</td>
<td>474</td>
<td>398</td>
<td>474</td>
<td>398</td>
<td>72</td>
<td>474</td>
<td>398</td>
<td>474</td>
<td>398</td>
<td>473</td>
<td>399</td>
<td>473</td>
<td>399</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>72</td>
<td>574</td>
<td>135</td>
<td>574</td>
<td>135</td>
<td>574</td>
<td>136</td>
<td>72</td>
<td>574</td>
<td>135</td>
<td>575</td>
<td>135</td>
<td>574</td>
<td>135</td>
<td>574</td>
<td>135</td>
</tr>
</tbody>
</table>

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.: 

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Oct-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base** = 204  
**SPECrate®2017_int_peak** = 213

### General Notes (Continued)

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Enabled
- SNC set to Enabled
- IMC Interleaving set to 1-way Interleave
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1be6e46a485a0011
running on linux-bo7k Wed Oct 23 14:32:21 2019

SUT (System Under Test) info as seen by some common utilities. For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
  2  "physical id"s (chips)
  72  "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                72
On-line CPU(s) list:   0-71
Thread(s) per core:    2
Core(s) per socket:    18
```

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

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</tr>
</thead>
</table>

**SPECrate®2017_int_base = 204**

**SPECrate®2017_int_peak = 213**

### Platform Notes (Continued)

- **Socket(s):** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
- **Stepping:** 6
- **CPU MHz:** 2200.000
- **CPU max MHz:** 3900.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 4400.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 25344K
- **NUMA node0 CPU(s):** 0-2,5,6,9,10,14,15,36-38,41,42,45,46,50,51
- **NUMA node1 CPU(s):** 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
- **NUMA node2 CPU(s):** 18-20,23,24,27,28,32,33,54-56,59,60,63,64,68,69
- **NUMA node3 CPU(s):** 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71

**Flags:**
- fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
- pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp
- lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
- aperfmpref perf_known_freq pm xcmov mt
- xsave pb xtrm xptr pdc pdc pcd dca sse4_1 sse4_2 x2apic miov popcnt
- tsc_deadline_timer aes xsave avx f16c rdrand lahlf_lm abm 3dnowprefetch cpuid_fault
- epb cat_13 cdp_13 invpcid-single intel_pinn mba tpr_shadow vmmi flexpriority ept
- vpid fsqgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
- avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
- xsaveopt xsaves xsave cqm_l1l cqm_occw_l1l cqm_mmms_total cqm_mmms_local
- ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epf hwp_pkg_req pku
- ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)

node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51

node 0 size: 192073 MB

node 0 free: 191734 MB

node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53

node 1 size: 193527 MB

node 1 free: 193050 MB

node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69

node 2 size: 193527 MB

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPEC CPU®2017 Integer Rate Result
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SPECrade®2017_int_base = 204
SPECrade®2017_int_peak = 213

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

node 2 free: 193303 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 57 62 65 66 67 70 71
node 3 size: 193525 MB
node 3 free: 193309 MB
node distances:
   node 0   1   2   3
   0: 10 11 21 21
   1: 11 10 21 21
   2: 21 21 10 11
   3: 21 21 11 10

From /proc/meminfo
MemTotal: 791197436 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
oS-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-bo7k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Speculation, IBPB, IBRS_FW
run-level 3 Oct 23 13:51

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 79G 146G 36% /

(Continued on next page)
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Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP220811SW

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
          | 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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==============================================================================
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==============================================================================
(Continued on next page)
## Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>Language</th>
<th>Compiler</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++</td>
<td>523.xalancbmk_r(peak)</td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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<tr>
<td>C++</td>
<td>520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)</td>
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</tr>
<tr>
<td>Fortran</td>
<td>548.exchange2_r(base, peak)</td>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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Cisco Systems
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>204</th>
</tr>
</thead>
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<tr>
<td>SPECrate®2017_int_peak</td>
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</tr>
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</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Oct-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Peak Compiler Invocation

C benchmarks (except as noted below):
```bash
icc -m64 -std=c11
502.gcc_r.icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

C++ benchmarks (except as noted below):
```bash
icpc -m64
523.xalancbmk_r.icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin
```

Fortran benchmarks:
```bash
ifort -m64
```

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -D_FILE_OFFSET_BITS=64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
```bash
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-fno-strict-overflow  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc
```

```bash
502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/je5.0.1-32/lib -ljemalloc
```

```bash
505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4
```

(Continued on next page)
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Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

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#### SPEC CPU 2017 Integer Rate Result

- **SPECrate®2017_int_base = 204**
- **SPECrate®2017_int_peak = 213**

### Peak Optimization Flags (Continued)

505.mcf_r (continued):
```bash
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

525.x264_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc`

557.xz_r: Same as 505.mcf_r

#### C++ benchmarks:

520.omnetpp_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc`

523.xalancbmk_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

#### Fortran benchmarks:

- `Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
- `L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

## SPEC CPU®2017 Integer Rate Result

### Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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