Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECrate®2017_fp_base = 193
SPECrate®2017_fp_peak = 196

Hardware
CPU Name: Intel Xeon Gold 5220
Max MHz: 3900
Nominal: 2200
Enabled: 36 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4g released Jul-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: default
# SPEC CPU®2017 Floating Point Rate Result

## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>72</td>
<td>1525</td>
<td>473</td>
<td>1525</td>
<td>473</td>
<td>1528</td>
<td>473</td>
<td>1528</td>
<td>473</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>72</td>
<td>579</td>
<td>157</td>
<td>579</td>
<td>157</td>
<td>578</td>
<td>158</td>
<td>579</td>
<td>157</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>72</td>
<td>461</td>
<td>148</td>
<td>462</td>
<td>148</td>
<td>462</td>
<td>148</td>
<td>460</td>
<td>149</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>72</td>
<td>1738</td>
<td>109</td>
<td>1733</td>
<td>109</td>
<td>1729</td>
<td>108</td>
<td>1734</td>
<td>109</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>72</td>
<td>769</td>
<td>219</td>
<td>769</td>
<td>219</td>
<td>767</td>
<td>219</td>
<td>769</td>
<td>219</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>72</td>
<td>683</td>
<td>111</td>
<td>683</td>
<td>111</td>
<td>683</td>
<td>111</td>
<td>683</td>
<td>111</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>72</td>
<td>805</td>
<td>201</td>
<td>798</td>
<td>202</td>
<td>798</td>
<td>202</td>
<td>788</td>
<td>205</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>72</td>
<td>545</td>
<td>201</td>
<td>544</td>
<td>202</td>
<td>544</td>
<td>202</td>
<td>545</td>
<td>201</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>72</td>
<td>563</td>
<td>224</td>
<td>562</td>
<td>224</td>
<td>561</td>
<td>225</td>
<td>548</td>
<td>230</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>72</td>
<td>399</td>
<td>449</td>
<td>398</td>
<td>450</td>
<td>398</td>
<td>450</td>
<td>399</td>
<td>449</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>72</td>
<td>384</td>
<td>316</td>
<td>380</td>
<td>319</td>
<td>384</td>
<td>316</td>
<td>383</td>
<td>317</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>72</td>
<td>1881</td>
<td>149</td>
<td>1882</td>
<td>149</td>
<td>1882</td>
<td>149</td>
<td>1881</td>
<td>149</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>72</td>
<td>1275</td>
<td>89.8</td>
<td>1273</td>
<td>89.9</td>
<td>1273</td>
<td>89.9</td>
<td>1280</td>
<td>89.4</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 193**

**SPECrate®2017_fp_peak = 196**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPECrates®
SPECrates®
SPECrate®2017_fp_base = 193
SPECrate®2017_fp_peak = 196

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbb1e6e46a485a0011
running on linux-bo7k Wed Oct 23 23:33:20 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
  2 "physical id"s (chips)
    72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores: 18
  siblings: 36
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 2
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_base</td>
<td>193</td>
</tr>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>196</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

CPU family:       6
Model:            85
Model name:       Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
Stepping:         6
CPU MHz:          2200.000
CPU max MHz:      3900.0000
CPU min MHz:      1000.0000
BogoMIPS:         4400.00
Virtualization:   VT-x
L1d cache:        32K
L1i cache:        32K
L2 cache:         1024K
L3 cache:         25344K
NUMA node0 CPU(s): 0-2, 5, 6, 9, 10, 14, 15, 36-38, 41, 42, 45, 46, 50, 51
NUMA node1 CPU(s): 3, 4, 7, 8, 11-13, 16, 17, 39, 40, 43, 44, 47-49, 52, 53
NUMA node2 CPU(s): 18-20, 24, 27, 29, 32, 33, 54-56, 59, 60, 63, 64, 68, 69
NUMA node3 CPU(s): 21, 22, 25, 26, 29-31, 34, 35, 57, 58, 61, 62, 65-67, 70, 71

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
       pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp
       lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
       aperfmperp tsc_known_freq pni pclmulqdq dtles64 monitor ds_cpl vmx smx est tm2 ssse3
       sdbg fma cx16 xtrp pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
       tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
       epb cat_13 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vmmi fxsaveopt ept
       vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2  erms invpcid rtm cmx mxp rdt_a
       avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
       xsavesopt xsaveopt xgetbv1 xsaves cmqm_llc cmqm_occup_llc cmqm_mbm_total cmqm_mbm_local
       ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
       ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
      cache size : 25344 KO

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
   node 0 size: 192073 MB
   node 0 free: 180852 MB
   node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
   node 1 size: 193527 MB
   node 1 free: 185574 MB
   node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
   node 2 size: 193527 MB
   node 2 free: 185826 MB
   node 3 cpus: 21 22 25 26 29 30 31 34 35 57 58 61 62 65 66 67 70 71
   node 3 size: 193525 MB

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPECrater®2017_fp_base = 193
SPECrater®2017_fp_peak = 196

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

node 3 free: 185834 MB
node distances:
  node 0 1 2 3
  0: 10 11 21 21
  1: 11 10 21 21
  2: 21 21 10 11
  3: 21 21 11 10

From /proc/meminfo
  MemTotal: 791197436 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-bo7k 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 23 13:51

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 110G 115G 49% /

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECrate\textsuperscript{®}2017\textsubscript{fp_base} = 193
SPECrate\textsuperscript{®}2017\textsubscript{fp_peak} = 196

Platform Notes (Continued)

Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP220811SW

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

C               | 519.lbm\textsubscript{r}(base, peak) 538.imagick\textsubscript{r}(base, peak) 544.nab\textsubscript{r}(base, peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++             | 508.namd\textsubscript{r}(base, peak) 510.parest\textsubscript{r}(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C          | 511.povray\textsubscript{r}(base, peak) 526.blender\textsubscript{r}(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactuBSSN\textsubscript{r}(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPECrate®2017_fp_base = 193
SPECrate®2017_fp_peak = 196

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
| 554.roma_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPECratre®2017_fp_base = 193
SPECratre®2017_fp_peak = 196

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPEC®2017 Floating Point Rate Result

SPECrate®2017_fp_base = 193
SPECrate®2017_fp_peak = 196

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)  
SPECrate®2017_fp_base = 193
SPECrate®2017_fp_peak = 196

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Oct-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
               -ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
            -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
            -qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
               -ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
               -ffinite-math-only -qopt-mem-layout-trans=4 -auto
               -nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
             -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
             -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
             -align array32byte

Benchmarks using both Fortran and C:
   -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
   -no-prec-div -qopt-prefetch -ffinite-math-only
   -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
   -align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
               -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
               -qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
               -ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
   -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)
## Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 193</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 196</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Oct-2019</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-10-23 14:03:19-0400.
Originally published on 2019-11-25.