Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeak®2017_fp_base</th>
<th>SPECspeak®2017_fp_peak</th>
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</thead>
<tbody>
<tr>
<td>217</td>
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</table>

**CPU2017 License**: 9019  
**Test Sponsor**: Cisco Systems  
**Tested by**: Cisco Systems  
**Test Date**: Oct-2019  
**Hardware Availability**: Apr-2019  
**Software Availability**: May-2019

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeak®2017_fp_base (217)</th>
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<tbody>
<tr>
<td>603.bwaves_s 112</td>
<td>0</td>
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<tr>
<td>607.cactuBSSN_s 112</td>
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<tr>
<td>619.lbm_s 112</td>
<td>149</td>
</tr>
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<td>621.wrf_s 112</td>
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<tr>
<td>627.cam4_s 112</td>
<td>181</td>
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<tr>
<td>628.pop2_s 112</td>
<td>50.5</td>
</tr>
<tr>
<td>638.imagick_s 112</td>
<td>274</td>
</tr>
<tr>
<td>644.nab_s 112</td>
<td>514</td>
</tr>
<tr>
<td>649.fotonik3d_s 112</td>
<td>118</td>
</tr>
<tr>
<td>654.roms_s 112</td>
<td>334</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name**: Intel Xeon Platinum 8280M  
- **Max MHz**: 4000  
- **Nominal**: 2700  
- **Enabled**: 112 cores, 4 chips  
- **Orderable**: 2, 4 Chips  
- **Cache L1**: 32 KB I + 32 KB D on chip per core  
- **L2**: 1 MB I+D on chip per core  
- **L3**: 38.5 MB I+D on chip per chip  
- **Other**: None  
- **Memory**: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage**: 1 x 600 GB 15K RPM SAS HDD  
- **Other**: None

**Software**

- **OS**: SUSE Linux Enterprise Server 15 (x86_64)  
- **Compiler**: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel**: Yes  
- **Firmware**: Version 4.0.3 released Mar-2019  
- **File System**: xfs  
- **System State**: Run level 3 (multi-user)  
- **Base Pointers**: 64-bit  
- **Peak Pointers**: Not Applicable  
- **Other**: None  
- **Power Management**: default
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Oct-2019
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
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<th>Base</th>
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</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 217
SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
SPEC CPU®2017 Floating Point Speed Result

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SPECspeed®2017_fp_base = 217
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011
running on linux-lozz Tue Oct 22 22:32:28 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8280M CPU @ 2.70GHz
  4 "physical id"s (chips)
112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
  28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
  28 29 30
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
  28 29 30
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
  28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8280M CPU @ 2.70GHz
Stepping: 6

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

Platform Notes (Continued)

CPU MHz: 2700.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-27
NUMA node1 CPU(s): 28-55
NUMA node2 CPU(s): 56-83
NUMA node3 CPU(s): 84-111
Flags: fpu vme de pse ts cmov pat mpx mre sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology

/proc/cpuinfo cache data
cache size : 39424 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 0 size: 385624 MB
node 0 free: 384885 MB
node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
node 1 size: 387056 MB
node 1 free: 386875 MB
node 2 cpus: 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
node 2 size: 387056 MB
node 2 free: 386875 MB
node 3 cpus: 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105
node 3 size: 387053 MB
node 3 free: 386844 MB

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

SPECspeed®2017_fp_base = 217
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Platform Notes (Continued)

node distances:
node  0  1  2  3
0:  10  21  21  21
1:  21  10  21  21
2:  21  21  10  21
3:  21  21  21  10

From /proc/meminfo
MemTotal:       1583884148 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-lozz 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault):       No status reported
Microarchitectural Data Sampling:          No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                         via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
                                         Speculation, IBPB, IBRS_FW

run-level 3 Oct 22 20:17

SPEC is set to: /home/cpu2017
    Filesystem     Type  Size  Used Avail Use% Mounted on
    /dev/sda2      xfs   273G   45G  229G  17% /

From /sys/devices/virtual/dmi/id
    BIOS:         Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
    Vendor:       Cisco

(Continued on next page)
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SPECspeed®2017_fp_base = 217
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Test Date: Oct-2019
Hardware Availability: Apr-2019
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Platform Notes (Continued)

Product: UCSC-C480-M5
Serial: FCH2227W00H

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
(Continued on next page)
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Tested by: Cisco Systems

Compilera Version Notes (Continued)

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

Base Compiler Invocation

- **C benchmarks:**
  ```
  icc -m64 -std=c11
  ```

- **Fortran benchmarks:**
  ```
  ifort -m64
  ```

- **Benchmarks using both Fortran and C:**
  ```
  ifort -m64 icc -m64 -std=c11
  ```

- **Benchmarks using Fortran, C, and C++:**
  ```
  icpc -m64 icc -m64 -std=c11 ifort -m64
  ```

Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>-DSPEC_LP64</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>-DSPEC_LP64</td>
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<tr>
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<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

Base Optimization Flags

- **C benchmarks:**
  ```
  -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
  ```

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8280M, 2.70GHz)  SPECspeed\textsuperscript{\textregistered}2017\textsubscript{\textsuperscript{fp base}} = 217
SPECspeed\textsuperscript{\textregistered}2017\textsubscript{\textsuperscript{fp peak}} = Not Run

CPU2017 License: 9019  Test Date: Oct-2019
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Base Optimization Flags (Continued)

C benchmarks (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC\_OPENMP

Fortran benchmarks:
-DSPEC\_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC\_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC\_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml