Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5222, 3.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

### SPECspeed®2017_fp_base = 94.5
SPECspeed®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (94.5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.0</td>
</tr>
<tr>
<td>20</td>
<td>20.0</td>
</tr>
<tr>
<td>50</td>
<td>50.0</td>
</tr>
<tr>
<td>80</td>
<td>80.0</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>120</td>
<td>120</td>
</tr>
<tr>
<td>140</td>
<td>140</td>
</tr>
<tr>
<td>160</td>
<td>160</td>
</tr>
<tr>
<td>180</td>
<td>180</td>
</tr>
<tr>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>220</td>
<td>220</td>
</tr>
<tr>
<td>240</td>
<td>240</td>
</tr>
<tr>
<td>260</td>
<td>260</td>
</tr>
<tr>
<td>280</td>
<td>280</td>
</tr>
<tr>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>320</td>
<td>320</td>
</tr>
<tr>
<td>340</td>
<td>340</td>
</tr>
<tr>
<td>360</td>
<td>360</td>
</tr>
<tr>
<td>380</td>
<td>380</td>
</tr>
<tr>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td>440</td>
<td>440</td>
</tr>
<tr>
<td>460</td>
<td>460</td>
</tr>
<tr>
<td>480</td>
<td>480</td>
</tr>
<tr>
<td>500</td>
<td>500</td>
</tr>
</tbody>
</table>

#### Hardware

**CPU Name:** Intel Xeon Gold 5222  
**Max MHz:** 3900  
**Nominal:** 3800  
**Enabled:** 16 cores, 4 chips  
**Orderable:** 2,4 Chips  
**Cache L1:** 32 KB I+ 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 16.5 MB I+D on chip per chip  
**Other:** None  
**Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
**Storage:** 1 x 300 GB 15K RPM SAS HDD  
**Other:** None

#### Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64)  
4.12.14-23-default  
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;  
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
**Parallel:** Yes  
**Firmware:** Version 4.0.3 released Mar-2019  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None  
**Power Management:** default
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603 bwaves_s</td>
<td>16</td>
<td>118</td>
<td>498</td>
<td>119</td>
<td>497</td>
<td>119</td>
<td>494</td>
</tr>
<tr>
<td>607 cactuBSSN_s</td>
<td>16</td>
<td>190</td>
<td><strong>87.6</strong></td>
<td>190</td>
<td>87.7</td>
<td>190</td>
<td>87.5</td>
</tr>
<tr>
<td>619 lbm_s</td>
<td>16</td>
<td>64.8</td>
<td>80.8</td>
<td>64.3</td>
<td>81.4</td>
<td>64.4</td>
<td><strong>81.3</strong></td>
</tr>
<tr>
<td>621 wrf_s</td>
<td>16</td>
<td>143</td>
<td>92.4</td>
<td><strong>143</strong></td>
<td><strong>92.5</strong></td>
<td>143</td>
<td>92.8</td>
</tr>
<tr>
<td>627 cam4_s</td>
<td>16</td>
<td>177</td>
<td>50.2</td>
<td>177</td>
<td>50.0</td>
<td>177</td>
<td><strong>50.1</strong></td>
</tr>
<tr>
<td>628 pop2_s</td>
<td>16</td>
<td>227</td>
<td>52.3</td>
<td><strong>230</strong></td>
<td><strong>51.6</strong></td>
<td>231</td>
<td>51.3</td>
</tr>
<tr>
<td>638 imagick_s</td>
<td>16</td>
<td>215</td>
<td><strong>67.1</strong></td>
<td>215</td>
<td>67.1</td>
<td>214</td>
<td>67.4</td>
</tr>
<tr>
<td>644 nab_s</td>
<td>16</td>
<td>144</td>
<td><strong>122</strong></td>
<td>144</td>
<td>121</td>
<td>144</td>
<td>122</td>
</tr>
<tr>
<td>649 fotoni3d_s</td>
<td>16</td>
<td>116</td>
<td>78.4</td>
<td><strong>113</strong></td>
<td><strong>80.6</strong></td>
<td>112</td>
<td>81.3</td>
</tr>
<tr>
<td>654 roms_s</td>
<td>16</td>
<td>161</td>
<td>97.8</td>
<td>154</td>
<td>102</td>
<td><strong>155</strong></td>
<td><strong>102</strong></td>
</tr>
</tbody>
</table>

**SPECspeed**\(^{2017\_fp\_base} = 94.5\)

**SPECspeed**\(^{2017\_fp\_peak} = \text{Not Run}\)

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5222, 3.80GHz)

SPECspeed®2017_fp_base = 94.5
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Oct-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbbie6e46a485a0011
running on linux-9yc8 Mon Oct 21 01:34:56 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
  4 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 2 5 9 13
  physical 1: cores 1 2 4 13
  physical 2: cores 2 5 8 13
  physical 3: cores 2 5 8 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5222 CPU @ 3.80GHz
Stepping: 6
CPU MHz: 3800.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 7600.00

(Continued on next page)
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

**Cisco UCS C480 M5 (Intel Xeon Gold 5222, 3.80GHz)**

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>94.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

<table>
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<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Platform Notes (Continued)

- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 16896K
- **NUMA node0 CPU(s):** 0-3
- **NUMA node1 CPU(s):** 4-7
- **NUMA node2 CPU(s):** 8-11
- **NUMA node3 CPU(s):** 12-15
- **Flags:** fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 rsb ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust mmcl hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

```
/proc/cpuinfo cache data
 cache size : 16896 KB
```

From `numactl --hardware` **WARNING:** a numactl 'node' might or might not correspond to a physical chip.

- **available:** 4 nodes (0-3)
- node 0 cpus: 0 1 2 3
- node 0 size: 385629 MB
- node 0 free: 385190 MB
- node 1 cpus: 4 5 6 7
- node 1 size: 387060 MB
- node 1 free: 386830 MB
- node 2 cpus: 8 9 10 11
- node 2 size: 387060 MB
- node 2 free: 383077 MB
- node 3 cpus: 12 13 14 15
- node 3 size: 387029 MB
- node 3 free: 386739 MB

<table>
<thead>
<tr>
<th>node distances:</th>
</tr>
</thead>
<tbody>
<tr>
<td>node 0 1 2 3</td>
</tr>
<tr>
<td>0: 10 21 21 21</td>
</tr>
<tr>
<td>1: 21 10 31 21</td>
</tr>
<tr>
<td>2: 21 31 10 21</td>
</tr>
<tr>
<td>3: 31 21 21 10</td>
</tr>
</tbody>
</table>

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5222, 3.80GHz) SPECspeed\textsuperscript{\textregistered}2017\_fp\_base = 94.5
SPECspeed\textsuperscript{\textregistered}2017\_fp\_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

Platform Notes (Continued)

From /proc/meminfo
- MemTotal: 1583902596 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
- NAME="SLES"
- VERSION="15"
- VERSION_ID="15"
- PRETTY_NAME="SUSE Linux Enterprise Server 15"
- ID="sles"
- ID_LIKE="suse"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
- Linux linux-9yc8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
- x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
- CVE-2018-3620 (L1 Terminal Fault): No status reported
- Microarchitectural Data Sampling: No status reported
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS\_FW

run-level 3 Oct 20 23:09

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
- BIOS: Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
- Vendor: Cisco
- Product: UCSC-C480-M5
- Serial: FCH2238W00E

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
**Platform Notes (Continued)**

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

**Compiler Version Notes**

<table>
<thead>
<tr>
<th>Platform</th>
<th>Compiler Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
<tr>
<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++, C, Fortran</td>
<td>607.cactuBSSN_s(base)</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
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<td></td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>Fortran</td>
<td>603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)</td>
</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
<tr>
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</tr>
<tr>
<td>Fortran, C</td>
<td>621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)</td>
</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=gnu11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=gnu11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=gnu11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-10-21 04:34:55-0400.
Originally published on 2019-11-25.