**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

**SPEC Speed 2017**

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.59</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License**: 9019

<table>
<thead>
<tr>
<th>Threads</th>
<th>600.perlbench_s</th>
<th>602.gcc_s</th>
<th>605.mcf_s</th>
<th>620.omnetpp_s</th>
<th>623.xalancbmk_s</th>
<th>625.x264_s</th>
<th>631.deepsjeng_s</th>
<th>641.leela_s</th>
<th>648.exchange2_s</th>
<th>657.xz_s</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
<td>48</td>
</tr>
<tr>
<td>Threads</td>
<td>6.45</td>
<td>9.22</td>
<td>12.1</td>
<td>6.74</td>
<td>11.8</td>
<td>13.6</td>
<td>5.22</td>
<td>4.54</td>
<td>15.8</td>
<td>22.5</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name**: Intel Xeon Gold 6226
- **Max MHz**: 3700
- **Nominal**: 2700
- **Enabled**: 48 cores, 4 chips
- **Orderable**: 2,4 Chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **Cache L2**: 1 MB I+D on chip per core
- **Cache L3**: 19.25 MB I+D on chip per chip
- **Memory**: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage**: 1 x 300 GB 15K RPM SAS HDD
- **Other**: None
- **Operating System**: SUSE Linux Enterprise Server 15 (x86_64)
- **OS Version**: 4.12.14-23-default
- **Compiler**: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux
- **Fortran**: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel**: Yes
- **Firmware**: Version 4.0.3 released Mar-2019
- **File System**: xfs
- **System State**: Run level 3 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: Not Applicable
- **Other**: jemalloc memory allocator V5.0.1
- **Power Management**: default
**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>48</td>
<td>275</td>
<td>6.45</td>
<td>277</td>
<td>6.40</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>48</td>
<td>436</td>
<td>9.13</td>
<td>432</td>
<td>9.22</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>48</td>
<td>393</td>
<td>12.0</td>
<td>390</td>
<td>12.1</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>48</td>
<td>238</td>
<td>6.84</td>
<td>242</td>
<td>6.73</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>48</td>
<td>120</td>
<td>11.8</td>
<td>120</td>
<td>11.8</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>48</td>
<td>130</td>
<td>13.6</td>
<td>130</td>
<td>13.6</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>48</td>
<td>274</td>
<td>5.23</td>
<td>274</td>
<td>5.22</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>48</td>
<td>376</td>
<td>4.54</td>
<td>376</td>
<td>4.53</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>48</td>
<td>186</td>
<td>15.8</td>
<td>188</td>
<td>15.7</td>
</tr>
<tr>
<td>657.z2_s</td>
<td>48</td>
<td>274</td>
<td>22.5</td>
<td>274</td>
<td>22.5</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_int_base = 9.59**

**SPECspeed®2017_int_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Operating System Notes**
Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

**General Notes**
Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPECspeed®2017_int_base = 9.59
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Date: Oct-2019
Test Sponsor: Cisco Systems
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbe6e46a485a0011
running on linux-lozz Sat Oct 12 22:08:12 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6226 CPU @ 2.70GHz
  4 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
physical 0: cores 0 2 3 4 5 6 8 9 10 11 12 13
physical 1: cores 0 2 3 4 5 6 8 9 10 11 13 14
physical 2: cores 0 2 3 4 6 8 9 10 11 12 13 14
physical 3: cores 0 2 3 5 6 8 9 10 11 12 13 14

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6226 CPU @ 2.70GHz
Stepping: 7
CPU MHz: 2700.000
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 5400.00

(Continued on next page)
## Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 19712K
NUMA node0 CPU(s): 0-11
NUMA node1 CPU(s): 12-23
NUMA node2 CPU(s): 24-35
NUMA node3 CPU(s): 36-47
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xgetbv1 xsaves cqmm11c cqmm2 occupancy llc cqmm2_total cqmm2_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
nodeno CPUs: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 385627 MB
node 0 free: 385102 MB
node 1 CPUs: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 387059 MB
node 1 free: 386885 MB
node 2 CPUs: 24 25 26 27 28 29 30 31 32 33 34 35
node 2 size: 387059 MB
node 2 free: 386822 MB
node 3 CPUs: 36 37 38 39 40 41 42 43 44 45 46 47
node 3 size: 387027 MB
node 3 free: 386769 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10
```

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 9.59
SPECspeed®2017_int_peak = Not Run

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 1583896512 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-lozz 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Oct 12 22:07
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 273G 41G 232G 16% /

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
Vendor: Cisco
Product: UCSC-C480-M5
Serial: FCH2227W00H

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)

SPECSpeed®2017_int_base = 9.59
SPECSpeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
  | 625.x264_s(base) 657.xz_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
  | 641.leela_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
Fortran  | 648.exchange2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
# SPEC CPU®2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS C480 M5 (Intel Xeon Gold 6226, 2.70GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>9.59</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

## Base Portability Flags

<table>
<thead>
<tr>
<th>Base Portability Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>602.gcc_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>605.mcf_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>620.omnetpp_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>625.x264_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>631.deepsjeng_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>641.leela_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>648.exchange2_s: -DSPEC_LP64</td>
</tr>
<tr>
<td>657.xz_s: -DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

**C benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc

**Fortran benchmarks:**  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:  

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

---

**SPEC CPU** and **SPECspeed** are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2019-10-13 01:08:11-0400.  
Originally published on 2019-11-25.