Lenovo Global Technology
ThinkSystem SR950
(2.30 GHz, Intel Xeon Gold 5218B)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Threads

<p>| | | | | | | | | | | | | | | | |</p>
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SPECspeed®2017_fp_base = 168
SPECspeed®2017_fp_peak = Not Run

**Hardware**

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<tr>
<td>CPU Name:</td>
<td>Intel Xeon Gold 5218B</td>
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<td>Max MHz:</td>
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<td>64 cores, 4 chips</td>
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<td>Cache L1:</td>
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<td>Memory:</td>
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<td>Storage:</td>
<td>1 x 800 GB SATA SSD</td>
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<td>Other:</td>
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**Software**

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<td>SUSE Linux Enterprise Server 15 (x86_64)</td>
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<td>Compiler:</td>
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<td>Parallel:</td>
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Lenovo Global Technology
ThinkSystem SR950
(2.30 GHz, Intel Xeon Gold 5218B)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2019 Standard Performance Evaluation Corporation

Lenovo Global Technology

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

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<td>2.68</td>
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</table>

SPECspeed®2017_fp_base = 168
SPECspeed®2017_fp_peak = Not Run

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017-1.1.0-ic19.0u4/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages disabled by default
echo never > /sys/kernel/mm/transparent_hugepage/enabled
echo never > /sys/kernel/mm/transparent_hugepage/defrag
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a)

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR950
(2.30 GHz, Intel Xeon Gold 5218B)

**General Notes (Continued)**

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

**Platform Notes**

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
CPU P-state Control set to Autonomous
Hyper-Threading set to Disable
Trusted Execution Technology set to Enable
DCU Streamer Prefetcher set to Disable
MONITOR/MWAIT set to Enable

Sysinfo program /home/cpu2017-1.1.0-ic19.0u4/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb1e6e46a485a0011
running on linux-ulb8 Fri Nov 8 12:36:15 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
4 "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR950
(2.30 GHz, Intel Xeon Gold 5218B)

SPECspeed®2017_fp_base = 168
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test Date: Nov-2019
Tested by: Lenovo Global Technology
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2300.000
BogoMIPS: 4600.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
NUMA node2 CPU(s): 32-47
NUMA node3 CPU(s): 48-63
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpic pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abrdi fmask falt uapa mcm cpb mfpub msr牝肋 GHz

/proc/cpuinfo cache data

cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 193118 MB
node 0 free: 189678 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 193486 MB
node 1 free: 193251 MB
node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 2 size: 193515 MB
node 2 free: 193225 MB
node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
node 3 size: 193512 MB
node 3 free: 192414 MB
node distances:
node 0 1 2 3

(Continued on next page)
Lenovo Global Technology

ThinkSystem SR950
(2.30 GHz, Intel Xeon Gold 5218B)

<table>
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<th>SPECspeed®2017_fp_peak</th>
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<tr>
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CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test Date: Nov-2019
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Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

0: 10 31 21 21
1: 31 10 21 21
2: 21 21 10 31
3: 21 21 31 10

From /proc/meminfo
MemTotal: 792199488 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-ulb8 4.12.14-25.13-default #1 SMP Tue Aug 14 15:07:35 UTC 2018 (947aa51) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Nov 8 10:10

SPEC is set to: /home/cpu2017-1.1.0-ic19.0u4
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 744G 75G 670G 10% /

From /sys/devices/virtual/dmi/id
BIOS: Lenovo -[PSE121R-1.53]- 07/03/2019
Vendor: Lenovo
Product: ThinkSystem SR950 -[7X12ABC1WW]-
Product Family: ThinkSystem

(Continued on next page)
**Lenovo Global Technology**

**ThinkSystem SR950**
*(2.30 GHz, Intel Xeon Gold 5218B)*

<table>
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**SPECspeed®2017_fp_base = 168**

**SPECspeed®2017_fp_peak = Not Run**

**Test Date:** Nov-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

---

**Platform Notes (Continued)**

Serial: none

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 48x NO DIMM NO DIMM
- 48x Samsung M393A2K43CB2-CVF 16 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

The marketing name for the processor in this result, which appears in the CPU name and hardware model areas, is different from sysinfo because a pre-production processor was used. The pre-production processor differs from the production processor in name only.

---

**Compiler Version Notes**

---

**C**

| 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base) |

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

**C++, C, Fortran**

| 607.cactuBSSN_s(base) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

**Fortran**

| 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base) |

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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(Continued on next page)
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| SPECspeed®2017_fp_base = | 168 |
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CPU2017 License: 9017
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Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
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CPU2017 License: 9017
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Hardware Availability: Apr-2019
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Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-F.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-F.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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