Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Platinum 8280, 2.70GHz)

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Platinum 8280</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64)</td>
</tr>
<tr>
<td>Max MHz: 4000</td>
<td>4.12.14-23-default</td>
</tr>
<tr>
<td>Nominal: 2700</td>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++</td>
</tr>
<tr>
<td>Enabled: 56 cores, 2 chips, 2 threads/core</td>
<td>Compiler for Linux;</td>
</tr>
<tr>
<td>Orderable: 1.2 Chips</td>
<td>Fortran: Version 19.0.4.227 of Intel Fortran</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>Compiler for Linux</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>L3: 38.5 MB I+D on chip per chip</td>
<td>Firmware: Version 4.0.4g released Jul-2019</td>
</tr>
<tr>
<td>Other: None</td>
<td>File System: btrfs</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Storage: 1 x 240 GB M.2 SATA SSD</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td></td>
<td>Other: jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td></td>
<td>Power Management: default</td>
</tr>
</tbody>
</table>

| SPECrate®2017_int_base = 339 |
| SPECrate®2017_int_peak = 356 |

| Test Date: Nov-2019 |
| Hardware Availability: Apr-2019 |
| Software Availability: May-2019 |

| Copies | 0 | 40.0 | 80.0 | 120 | 160 | 200 | 240 | 280 | 320 | 360 | 400 | 440 | 480 | 520 | 560 | 600 | 640 | 680 | 720 | 760 | 800 |
|--------|---|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 500.perlbench_r | 112 | 310 | 310 | 269 | 257 | 235 |
| 502.gcc_r | 112 | 423 | 421 | 395 |
| 505.mcf_r | 112 | 202 | 202 |
| 520.omnetpp_r | 112 | 342 | 342 |
| 523.xalancbmk_r | 112 | 727 |
| 525.x264_r | 112 | 763 |
| 531.deepsjeng_r | 112 | 294 |
| 541.leela_r | 112 | 282 |
| 548.exchange2_r | 112 | 725 |
| 557.xz_r | 112 | 227 |

SPECrate®2017_int_base (339) SPECrate®2017_int_peak (356)
Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Platinum 8280, 2.70GHz)

SPEC CPU®2017 Integer Rate Result

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Cisco Systems

SPECrate®2017_int_base = 339

SPECrate®2017_int_peak = 356

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2019
Hardware Availability: Apr-2019
Tested by: Cisco Systems
Software Availability: May-2019

Results Table

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<thead>
<tr>
<th>Benchmark</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>112</td>
<td>663</td>
<td>269</td>
<td>658</td>
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<td>310</td>
<td>112</td>
<td>575</td>
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<tr>
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<td>634</td>
<td>250</td>
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<td>258</td>
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<td>520.omnetpp_r</td>
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<td>729</td>
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<td>727</td>
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<tr>
<td>523.xalancbmk_r</td>
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<td>525.x264_r</td>
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<tr>
<td>548.exchange2_r</td>
<td>112</td>
<td>405</td>
<td>725</td>
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<tr>
<td>557.xz_r</td>
<td>112</td>
<td>532</td>
<td>227</td>
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<td>227</td>
<td>533</td>
<td>227</td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 339
SPECrate®2017_int_peak = 356

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
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SPECrate®2017_int_base = 339
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011
running on linux-cud8 Wed Nov 6 20:28:28 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
  2 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Hardware Availability: Apr-2019
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Platform Notes (Continued)

Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8280 CPU @ 2.70GHz
Stepping: 7
CPU MHz: 2700.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-3,7-9,14-17,21-23,56-59,63-65,70-73,77-79
NUMA node1 CPU(s): 4-6,10-13,18-20,24-27,60-62,66-69,74-76,80-83
NUMA node2 CPU(s): 28-31,35-37,42-45,49-51,84-87,91-93,98-101,105-107
NUMA node3 CPU(s): 32-34,38-41,46-48,52-55,88-90,94-97,102-104,108-111
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
	
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdrp l1vpcid_single intel_pinn mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 0rns invvpce rtm cmmp mxp rdts
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt
	
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
table
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78
from: 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78
node 0 size: 192072 MB
node 0 free: 191682 MB
node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81
82 83

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2019
Hardware Availability: Apr-2019
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Platform Notes (Continued)

node 1 size: 193525 MB
node 1 free: 193053 MB
node 2 cpus: 28 29 30 31 35 36 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100 101 105 106 107
node 2 size: 193525 MB
node 2 free: 193284 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 88 89 90 94 95 96 97 102 103 104 108 109 110 111
node 3 size: 193522 MB
node 3 free: 193286 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791189876 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling:
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

(Continued on next page)
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Platform Notes (Continued)

run-level 3 Nov 6 20:24

SPEC is set to: /home/cpu2017
     Filesystem   Type  Size  Used  Avail  Use%  Mounted on
     /dev/sda2    btrfs  224G   38G   186G  17%   /home

From /sys/devices/virtual/dmi/id
     BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
     Vendor: Cisco Systems Inc
     Product: UCSC-C220-M5SX
     Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
     24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416

(Continued on next page)
Cisco Systems
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<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Nov-2019</th>
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<tr>
<td>Test Sponsor: Cisco Systems</td>
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<td>Tested by:Cisco Systems</td>
<td>Software Availability: May-2019</td>
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</tbody>
</table>

**Compiler Version Notes (Continued)**

---

```plaintext
C  | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
   | 525.x264_r(base, peak) 557.xz_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++ | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++ | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
     | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)
Fortran | 548.exchange2_r (base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)
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Base Optimization Flags (Continued)

C++ benchmarks (continued):
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

Fortran benchmarks:
- W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
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Tested by: Cisco Systems

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Software Availability: May-2019

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
# SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Platinum 8280, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tbody>
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<td>339</td>
<td>356</td>
</tr>
</tbody>
</table>

**Cisco Systems**

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Nov-2019

Hardware Availability: Apr-2019

Software Availability: May-2019

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.


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