Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5215M, 2.50GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
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<tr>
<th>SPECrate®2017_fp_base =</th>
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<tbody>
<tr>
<td>SPECrate®2017_fp_peak =</td>
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Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

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<td>549.fotonik3d_r 80</td>
<td>245</td>
</tr>
<tr>
<td>554.roms_r 80</td>
<td>128</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 5215M
Max MHz: 3400
Nominal: 2500
Enabled: 40 cores, 4 chips, 2 threads/core
Orderable: 2, 4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 13.75 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.3 released Mar-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: default
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5215M, 2.50GHz)

CPU2017 License: 9019
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SPECrate®2017_fp_base = 246
SPECrate®2017_fp_peak = Not Run

Results Table

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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5215M, 2.50GHz)

**SPECrater®2017 fp_base** = 246

**SPECrater®2017 fp_peak** = Not Run

---

**General Notes (Continued)**

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6a46e485a0011
running on linux-mz3p Thu Nov 7 07:33:00 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz
4 "physical id"s (chips)
80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
physical 2: cores 0 1 2 3 4 8 9 10 11 12
physical 3: cores 0 1 2 3 4 8 9 10 11 12

From lsccpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0–79
Thread(s) per core: 2
Core(s) per socket: 10

(Continued on next page)
**Platform Notes (Continued)**

Socket(s): 4  
NUMA node(s): 4  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Gold 5215M CPU @ 2.50GHz  
Stepping: 6  
CPU MHz: 2500.000  
CPU max MHz: 3400.0000  
CPU min MHz: 1000.0000  
BogoMIPS: 5000.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 14080K  
NUMA node0 CPU(s): 0-9,40-49  
NUMA node1 CPU(s): 10-19,50-59  
NUMA node2 CPU(s): 20-29,60-69  
NUMA node3 CPU(s): 30-39,70-79  
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg xsave aes xsaveopt avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vmi xmppriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cf avx512bw avx512vl xsaveopt xsavec xgetbv1 xsave xsaveopt xsaves cqm_llc cqm_occ OPP cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_kgg req pku ospk make avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49  
node 0 size: 385597 MB  
node 0 free: 379149 MB  
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59  
node 1 size: 387057 MB  
node 1 free: 382606 MB  
node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69  
node 2 size: 387057 MB
### Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 5215M, 2.50GHz)

<table>
<thead>
<tr>
<th>Platform Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>node 2 free: 382611 MB</td>
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<tr>
<td>node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79</td>
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<tr>
<td>node 3 size: 387055 MB</td>
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<tr>
<td>node 3 free: 382578 MB</td>
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<td>node distances:</td>
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<td>0: 10 21 21 31</td>
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<tr>
<td>1: 21 10 31 21</td>
</tr>
<tr>
<td>2: 21 31 10 21</td>
</tr>
<tr>
<td>3: 31 21 21 10</td>
</tr>
</tbody>
</table>

From `/proc/meminfo`
- MemTotal: 1583890300 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release*` /`/etc/*version*`
- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
- Linux linux-mz3p 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
- x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
- CVE-2018-3620 (L1 Terminal Fault): No status reported
- Microarchitectural Data Sampling: No status reported
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Nov 7 03:01

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 xfs 549G 102G 448G 19% /
Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
    BIOS:  Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
    Vendor:  Cisco
    Product: UCSC-C480-M5
    Serial:  FCH2238W019

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:  48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base) |
|-------------------------------|-------------|-------------|-------------|
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
|-------------------------------|-------------|-------------|-------------|

==============================================================================
| C++             | 508.namd_r(base) 510.parest_r(base) |
|-------------------------------|-------------|-------------|-------------|
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
|-------------------------------|-------------|-------------|-------------|

==============================================================================
| C++, C          | 511.povray_r(base) 526.blender_r(base) |
|-------------------------------|-------------|-------------|-------------|
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, |
| Version 19.0.4.227 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
|-------------------------------|-------------|-------------|-------------|

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(Continued on next page)
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Compiler Version Notes (Continued)

C++, C, Fortran | 507.cactuBSSN_r(base)  
------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

------------------------------------------------------------------
Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)  
------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

------------------------------------------------------------------
Fortran, C | 521.wrf_r(base) 527.cam4_r(base)  
------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
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Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  

Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

C++ benchmarks:  
icpc -m64

Fortran benchmarks:  
ifort -m64

Benchmarks using both Fortran and C:  
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Cisco Systems
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Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: –DSPEC_LP64
507.cactuBSSN_r: –DSPEC_LP64
508.namd_r: –DSPEC_LP64
510.parest_r: –DSPEC_LP64
511.povray_r: –DSPEC_LP64
519.lbm_r: –DSPEC_LP64
521.wrf_r: –DSPEC_LP64 –DSPEC_CASE_FLAG –convert big_endian
526.blender_r: –DSPEC_LP64 –DSPEC_LINUX –funsigned-char
527.cam4_r: –DSPEC_LP64 –DSPEC_CASE_FLAG
538.imagick_r: –DSPEC_LP64
544.nab_r: –DSPEC_LP64
549.fotonik3d_r: –DSPEC_LP64
554.roms_r: –DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 –ipo -03 –no-prec-div –qopt-prefetch
-ffinite-math-only –qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 –ipo -03 –no-prec-div –qopt-prefetch
-ffinite-math-only –qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 –ipo -03 –no-prec-div –qopt-prefetch
-ffinite-math-only –qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 –ipo -03 –no-prec-div –qopt-prefetch
-ffinite-math-only –qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

(Continued on next page)
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### Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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