## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS B480 M5 (Intel Xeon Gold 6248, 2.50GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>186</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
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**CPU2017 License:** 9019  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

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<thead>
<tr>
<th>Threads</th>
<th>603.bwaves_s</th>
<th>80</th>
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<tr>
<td></td>
<td></td>
<td>211</td>
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<tr>
<td></td>
<td>607.cactuBSSN_s</td>
<td>80</td>
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<tr>
<td></td>
<td>619.lbm_s</td>
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<tr>
<td></td>
<td>621.wrf_s</td>
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<td>627.cam4_s</td>
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<td>628.pop2_s</td>
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<tr>
<td></td>
<td>638.imagick_s</td>
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<tr>
<td></td>
<td>644.nab_s</td>
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<tr>
<td></td>
<td>649.fotonik3d_s</td>
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<tr>
<td></td>
<td>654.roms_s</td>
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| SPECspeed®2017_fp_base (186) |

### Hardware

**CPU Name:** Intel Xeon Gold 6248  
**Max MHz:** 3900  
**Nominal:** 2500  
**Enabled:** 80 cores, 4 chips  
**Orderable:** 2.4 Chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 27.5 MB I+D on chip per chip  
**Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
**Storage:** 1 x 1.9 TB SSD SAS  
**Other:** None

### Software

**OS:** SUSE Linux Enterprise Desktop 15 (x86_64)  
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
**Parallel:** Yes  
** Firmware:** Version 4.0.4b released Apr-2019  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None  
**Power Management:** default
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6248, 2.50GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed\(^{\text{2017_fp_base}}\) = 186
SPECspeed\(^{\text{2017_fp_peak}}\) = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>603.bwaves_s</td>
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<td>254</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed81e6e46a485a0011
running on linux-0enh Wed Oct 30 01:31:55 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
  4 "physical id"s (chips)
  80 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following
  excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 20
  siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 2: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 3: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
  Architecture:           x86_64
  CPU op-mode(s):         32-bit, 64-bit
  Byte Order:             Little Endian
  CPU(s):                 80
  On-line CPU(s) list:    0-79
  Thread(s) per core:     1
  Core(s) per socket:     20
  Socket(s):              4
  NUMA node(s):           4
  Vendor ID:              GenuineIntel
  CPU family:             6
  Model:                  85
  Model name:             Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
  Stepping:               6
  CPU MHz:                2500.000
  CPU max MHz:            3900.0000
  CPU min MHz:            1000.0000
  BogoMIPS:               5000.00

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6248, 2.50GHz)

CPU2017 License: 9019
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Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECspeed\textsuperscript{\textregistered}2017\_fp\_base = 186
SPECspeed\textsuperscript{\textregistered}2017\_fp\_peak = \textit{Not Run}

Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
NUMA node2 CPU(s): 40-59
NUMA node3 CPU(s): 60-79
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cdp_l3 invpcid_single intel_pwp mda tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid rlmsp cx16 smep bmi2 ibrms invpcid rbms invpcid ssbd

/platforminfo cache data
  cache size : 28160 KB
From numaclt --hardware WARNING: a numaclt 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
    node 0 size: 385467 MB
    node 0 free: 385113 MB
    node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
    node 1 size: 387057 MB
    node 1 free: 386858 MB
    node 2 cpus: 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
    node 2 size: 387057 MB
    node 2 free: 382811 MB
    node 3 cpus: 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
    node 3 size: 387026 MB
    node 3 free: 386845 MB
    node distances:
      node 0 1 2 3
        0: 10 21 21 21
        1: 21 10 21 21
        2: 21 21 10 21
        3: 21 21 21 10

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Platform Notes (Continued)

From /proc/meminfo
MemTotal: 1583727316 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
    os-release:
        NAME="SLED"
        VERSION="15"
        VERSION_ID="15"
        PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
        ID="sled"
        ID_LIKE="suse"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sled:15"

uname -a:
    Linux linux-0enh 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
    via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted
    Speculation, IBPB, IBRS_FW

run-level 3 Oct 29 23:13
SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
    Vendor: Cisco Systems Inc
    Product: UCSB-B480-M5
    Serial: FLM2230020U

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

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Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.