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<td>602.gcc_s</td>
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<tr>
<td>620.omnetpp_s</td>
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<tr>
<td>623.xalancbmk_s</td>
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<tr>
<td>625.x264_s</td>
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</tr>
<tr>
<td>631.deepsjeng_s</td>
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<tr>
<td>641.leela_s</td>
<td></td>
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<tr>
<td>648.exchange2_s</td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Platinum 8256
- **Max MHz:** 3900
- **Nominal:** 3800
- **Enabled:** 16 cores, 4 chips
- **Orderable:** 2, 4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240 GB M.2 SATA SSD
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** default
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**
Cisco UCS B480 M5 (Intel Xeon Platinum 8256, 3.80GHz)

### SPECspeed®2017_int_base =
### SPECspeed®2017_int_peak =

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Nov-2019  
**Hardware Availability:** Apr-2019  
**Tested by:** Cisco Systems  
**Software Availability:** May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

### Results Table

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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8256, 3.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)

sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6.75 of 2019-08-21 295195f888a3d7edbl6e646a485a0011
running on linux-icbf Mon Nov 4 17:29:05 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8256 CPU @ 3.80GHz
  4 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 0 9 11 13

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.
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</tbody>
</table>

Platform Notes (Continued)

```
tsc_deadline_timer aes xsave avx f16c sram lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ipt mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 file aes2mp bmi2 erms invpcid rtm cqmx pq xdi qd
rdsd pbseed fpx smx clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt xsaveopt
```

```
/proc/cpuinfo cache data
```

```
cache size : 16896 KB
```

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
```

```
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3
node 0 size: 387631 MB
node 0 free: 386316 MB
node 1 cpus: 4 5 6 7
node 1 size: 386852 MB
node 1 free: 386256 MB
node 2 cpus: 8 9 10 11
node 2 size: 386812 MB
node 2 free: 386256 MB
node 3 cpus: 12 13 14 15
node 3 size: 386758 MB
node 3 free: 386256 MB
node distances:
```

```
node distances:
```

```
node distances:
```

```
From /proc/meminfo
```

```
MemTotal: 1583904288 kB
```

```
HugePages_Total: 0
```

```
Hugepagesize: 2048 kB
```

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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| CPU2017 License: 9019 |
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**Platform Notes (Continued)**

Serial: FLM230102QU

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

**Compiler Version Notes**

<table>
<thead>
<tr>
<th>C</th>
<th>600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)</th>
</tr>
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<tbody>
<tr>
<td></td>
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</tr>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
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<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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<th>648.exchange2_s(base)</th>
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Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8256, 3.80GHz)

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SPECF has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbm_s: -DSPEC_LP64 -DSPEC_LINUX -DSPEC_LP64
624.deepsjeng_s: -DSPEC_LP64
641.perl_s: -DSPEC_LP64
643.x264_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

(Continued on next page)
SPECGPCPU®2017 Integer Speed Result

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Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8256, 3.80GHz) SPECspeed®2017_int_base = SPECspeed®2017_int_peak =

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### Base Optimization Flags (Continued)

C++ benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompilers/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

Fortran benchmarks:
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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