**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>Specrate®2017_int_base</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Specrate®2017_int_peak</td>
<td>243</td>
</tr>
</tbody>
</table>

- **CPU2017 License**: 9019
- **Test Date**: Nov-2019
- **Test Sponsor**: Cisco Systems
- **Hardware Availability**: Apr-2019
- **Tested by**: Cisco Systems
- **Software Availability**: May-2019

### Hardware
- **CPU Name**: Intel Xeon Gold 6240
- **Max MHz**: 3900
- **Nominal**: 2600
- **Enabled**: 36 cores, 2 chips, 2 threads/core
- **Orderable**: 1.2 Chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **L2**: 1 MB I+D on chip per core
- **L3**: 24.75 MB I+D on chip per chip
- **Memory**: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage**: 1 x 1.9 TB SSD SAS
- **Other**: None

### Software
- **OS**: SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler**: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel**: No
- **Firmware**: Version 4.0.4J released Aug-2019
- **File System**: xfs
- **System State**: Run level 3 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: 32/64-bit
- **Other**: jemalloc memory allocator V5.0.1
- **Power Management**: --

### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Program</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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</thead>
<tbody>
<tr>
<td>perlbench_r</td>
<td>72</td>
<td>207</td>
<td>243</td>
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<tr>
<td>gcc_r</td>
<td>72</td>
<td>185</td>
<td>215</td>
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<tr>
<td>mcf_r</td>
<td>72</td>
<td>149</td>
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<tr>
<td>omnetpp_r</td>
<td>72</td>
<td>254</td>
<td>304</td>
</tr>
<tr>
<td>xalancbmk_r</td>
<td>72</td>
<td>278</td>
<td>303</td>
</tr>
<tr>
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<td>457</td>
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<tr>
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<tr>
<td>exchange2_r</td>
<td>72</td>
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<tr>
<td>xz_r</td>
<td>72</td>
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

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<tr>
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<td>196</td>
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<tr>
<td>541.leela_r</td>
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<td>644</td>
<td>185</td>
<td>640</td>
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<td>634</td>
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<td>153</td>
<td>510</td>
<td>153</td>
<td>510</td>
<td>152</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)  

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</tr>
</tbody>
</table>

General Notes (Continued)

```
numactl --interleave=all runcpu <etc>
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011
running on linux-3c6s Fri Nov 15 11:25:41 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
  2 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
```

From lscpu:
```
Architecture:          x86_64
CPU op-mode(s):         32-bit, 64-bit
Byte Order:             Little Endian
CPU(s):                 72
On-line CPU(s) list:    0-71
Thread(s) per core:     2
Core(s) per socket:     18
```
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPEC CPU®2017 Integer Rate Result
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Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-2,5,9,10,14,15,36-38,41,42,45,46,50,51
NUMA node1 CPU(s): 3,4,7,8,11-13,16,17,39,40,43,44,47-49,52,53
NUMA node2 CPU(s): 18-20,23,24,27,28,32,33,34,35,57,58,61,62,65-67,70,71
NUMA node3 CPU(s): 21,22,25,26,29-31,34,35,57,58,61,62,65-67,70,71
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbs gca x86_64 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_perf tsc xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_i3 cdp_l3 invpcid_single intel_pinn mba tpr_shadow vmx f1enable ept
vpid fsgrbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx ptt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xgetbv1 xsaves cqm_llc cqm_occ_all cqm_mbb_total cqm_mbb_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 9 10 14 15 36 37 38 41 42 45 46 50 51
node 0 size: 192074 MB
node 0 free: 191737 MB
node 1 cpus: 3 4 7 8 11 12 13 16 17 39 40 43 44 47 48 49 52 53
node 1 size: 195327 MB
node 1 free: 193177 MB
node 2 cpus: 18 19 20 23 24 27 28 32 33 54 55 56 59 60 63 64 68 69
node 2 size: 193527 MB

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

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Platform Notes (Continued)

node 2 free: 193149 MB
node 3 cpus: 21 22 25 26 29 30 31 34 35 57 61 62 65 66 67 70 71
node 3 size: 193525 MB
node 3 free: 193292 MB
node distances:
node 0 1 2 3
0:  10 11 21 21
1:  11 10 21 21
2:  21 21 10 11
3:  21 21 11 10

From /proc/meminfo
MemTotal:       791198344 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Nov 15 11:22

SPEC is set to: /home/cpu2017
Filesystem  Type  Size  Used Avail Use% Mounted on
/dev/sdq1    xfs   224G  40G  185G  18%  /

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

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Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5SX
Serial: WZP221106LZ

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base, peak)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 523.xalancbmk_r(peak)
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
  531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++ | 523.xalancbmk_r(peak)
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
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==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 548.exchange2_r(base, peak)
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---
# SPEC CPU®2017 Integer Rate Result

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## Base Compiler Invocation

- **C benchmarks:**
  - `icc -m64 -std=c11`

- **C++ benchmarks:**
  - `icpc -m64`

- **Fortran benchmarks:**
  - `ifort -m64`

## Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

- **C benchmarks:**
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  - `-qopt-mem-layout-trans=4`  
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
  - `-lqkmalloc`

- **C++ benchmarks:**
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  - `-qopt-mem-layout-trans=4`  
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
  - `-lqkmalloc`

- **Fortran benchmarks:**
  - `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`  
  - `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`  
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
  - `-lqkmalloc`
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

**SPECr®2017_int_base = 233**
**SPECr®2017_int_peak = 243**

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**Test Date:** Nov-2019
**Hardware Availability:** Apr-2019
**Software Availability:** May-2019

---

### Peak Compiler Invocation

C benchmarks (except as noted below):

- icc -m64 -std=c11


C++ benchmarks (except as noted below):

- icpc -m64

- 523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:

- ifort -m64

### Peak Portability Flags

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
- 502.gcc_r: -D_FILE_OFFSET_BITS=64
- 505.mcf_r: -DSPEC_LP64
- 520.omnetpp_r: -DSPEC_LP64
- 523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
- 525.x264_r: -DSPEC_LP64
- 531.deepsjeng_r: -DSPEC_LP64
- 541.leela_r: -DSPEC_LP64
- 548.exchange2_r: -DSPEC_LP64
- 557.xz_r: -DSPEC_LP64

### Peak Optimization Flags

C benchmarks:

- 500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

- 502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc

- 505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Nov-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 233**

**SPECrate®2017_int_peak = 243**

### Peak Optimization Flags (Continued)

505.mcf_r (continued):
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
- `-lqkmalloc`


557.xz_r: Same as 505.mcf_r

**C++ benchmarks:**


523.xalancbmk_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc`

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

**Fortran benchmarks:**


The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240, 2.60GHz)

SPECrate®2017_int_base = 233
SPECrate®2017_int_peak = 243

CPU2017 License: 9019
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Test Date: Nov-2019
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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