# SPEC CPU®2017 Floating Point Rate Result

**Dell Inc.**

PowerEdge M640 (Intel Xeon Gold 5217, 3.00GHz)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tr>
<td>503.bwaves_r</td>
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<tr>
<td>507.cactuBSSN_r</td>
<td>64</td>
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<tr>
<td>508.namd_r</td>
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<tr>
<td>554.roms_r</td>
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</tbody>
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## Hardware

- **CPU Name:** Intel Xeon Gold 5217
- **Max MHz:** 3700
- **Nominal:** 3000
- **Enabled:** 32 cores, 4 chips, 2 threads/core
- **Orderable:** 1,2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per core
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

## Software

- **OS:** Ubuntu 18.04.2 LTS
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux
- **Parallel:** No
- **Firmware:** Version 2.2.9 released May-2019
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --
SPEC CPU®2017 Floating Point Rate Result

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Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5217, 3.00GHz)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 202

Results Table

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</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation

(Continued on next page)
Dell Inc.
PowerEdge M640 (Intel Xeon Gold 5217, 3.00GHz)

**SPECrater®2017_fp_base = 198**
**SPECrater®2017_fp_peak = 202**

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  

**Test Date:** Mar-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

---

**General Notes (Continued)**

Filesystem page cache synced and cleared with:
```bash
sync; echo 3>/proc/sys/vm/drop_caches
```
runcpu command invoked through numactl i.e.:
```bash
numactl --interleave=all runcpu <etc>
```

---

**Platform Notes**

BIOS settings:  
ADDDC setting disabled  
Sub NUMA Cluster enabled  
Virtualization Technology disabled  
DCU Streamer Prefetcher enabled  
System Profile set to Custom  
CPU Performance set to Maximum Performance  
C States set to Autonomous  
C1E disabled  
Uncore Frequency set to Dynamic  
Energy Efficiency Policy set to Performance  
Memory Patrol Scrub disabled  
Logical Processor enabled  
PCI ASPM L1 Link Power Management disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9  
running on intel-sut Tue Nov 19 05:27:45 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
[https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5217 CPU @ 3.00GHz
4 "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
physical 2: cores 0 1 2 3 4 5 6 7
physical 3: cores 0 1 2 3 4 5 6 7
```

From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
```

(Continued on next page)
Dell Inc.

PowerEdge M640 (Intel Xeon Gold 5217, 3.00GHz)

CPU2017 License: 55  
Test Sponsor: Dell Inc.  
Tested by: Dell Inc.

SPECraten\textsuperscript{2017}_fp_peak = 202

<table>
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</tr>
</thead>
</table>

Platform Notes (Continued)


\begin{verbatim}
CPU(s): 64  
on-line CPU(s) list: 0-63  
Thread(s) per core: 2  
Core(s) per socket: 8  
Socket(s): 4  
NUMA node(s): 4  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85  
Model name: Intel(R) Xeon(R) Gold 5217 CPU @ 3.00GHz  
Stepping: 6  
CPU MHz: 3453.562  
BogoMIPS: 6000.00  
Virtualization: VT-x  
L1c cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 11264K  
NUMA node0 CPU(s): 0,4,8,12,16,20,24,28,32,36,40,44,48,52,56,60  
NUMA node1 CPU(s): 1,5,9,13,17,21,25,29,33,37,41,45,49,53,57,61  
NUMA node2 CPU(s): 2,6,10,14,18,22,26,30,34,38,42,46,50,54,58,62  
NUMA node3 CPU(s): 3,7,11,15,19,23,27,31,35,39,43,47,51,55,59,63  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acp1 mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good ntop tscSCALE nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt ioport ms save axx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault ebpx cat_l3 cdp_l3 invpcid_single intel_pinn ssbd mbb ibbp stibp ibrs_enhanced tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmx mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occsp llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni flush_l1d arch_capabilities

/proc/cpuinfo cache data
    cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60
    node 0 size: 192859 MB
    node 0 free: 192149 MB
    node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61
    node 1 size: 193532 MB
    node 1 free: 193011 MB
    node 2 cpus: 2 6 10 14 18 22 26 30 34 38 42 46 50 54 58 62

(Continued on next page)
\end{verbatim}
Platform Notes (Continued)

node 2 size: 193511 MB
node 2 free: 192978 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63
node 3 size: 193531 MB
node 3 free: 192897 MB
node distances:
node 0 1 2 3
  0: 10 21 31 21
  1: 21 10 21 31
  2: 31 21 10 21
  3: 21 31 21 10

From /proc/meminfo
 MemTotal: 791998640 kB
 HugePages_Total: 0
 Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
 Ubuntu 18.04.2 LTS

From /etc/*release* /etc/*version*
 debian_version: buster/sid
 os-release:
  NAME="Ubuntu"
  VERSION="18.04.2 LTS (Bionic Beaver)"
  ID=ubuntu
  ID_LIKE=debian
  PRETTY_NAME="Ubuntu 18.04.2 LTS"
  VERSION_ID="18.04"
  HOME_URL="https://www.ubuntu.com/
  SUPPORT_URL="https://help.ubuntu.com/

uname -a:
 Linux intel-sut 4.15.0-45-generic #48-Ubuntu SMP Tue Jan 29 16:28:13 UTC 2019 x86_64
 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB

run-level 3 Nov 18 21:35

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 ext4 439G 31G 386G 8% /

(Continued on next page)
Dell Inc.  
PowerEdge M640 (Intel Xeon Gold 5217, 3.00GHz)  

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 198</th>
<th>SPECrate®2017_fp_peak = 202</th>
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<tr>
<td><strong>CPU2017 License:</strong> 55</td>
<td><strong>Test Date:</strong> Mar-2019</td>
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<td><strong>Test Sponsor:</strong> Dell Inc.</td>
<td><strong>Hardware Availability:</strong> Apr-2019</td>
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<td><strong>Tested by:</strong> Dell Inc.</td>
<td><strong>Software Availability:</strong> May-2019</td>
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</tbody>
</table>

### Platform Notes (Continued)

Additional information from `dmidecode` follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **BIOS:** Dell Inc. 2.2.9 05/08/2019
- **Memory:**
  - 16x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2666
  - 8x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2666
  - 24x Not Specified Not Specified

(End of data from `sysinfo` program)

### Compiler Version Notes

C

<table>
<thead>
<tr>
<th>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</th>
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.

C++

| 508.namd_r(base, peak) 510.parest_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.

C++, C

| 511.povray_r(base, peak) 526.blender_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.

C++, C, Fortran

| 507.cactuBSSN_r(base, peak) |

(Continued on next page)
Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
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------------------------------------------------------------------------------
==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11
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Dell Inc.                    SPECrate®2017_fp_base = 198
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Hardware Availability: Apr-2019
Software Availability: May-2019

Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

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</table>

### Base Optimization Flags (Continued)

Benchmarks using both C and C++:
- -xCORE-AVX2
- -ipo
- -O3
- -no-prec-div
- -qopt-prefetch
- -ffinite-math-only
- -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
- -xCORE-AVX2
- -ipo
- -O3
- -no-prec-div
- -qopt-prefetch
- -ffinite-math-only
- -qopt-mem-layout-trans=4
- -auto
- -nostandard-realloc-lhs
- -align array32byte

### Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:

```
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:

```
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4
```

(Continued on next page)
Peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only

(Continued on next page)
Dell Inc.  

PowerEdge M640 (Intel Xeon Gold 5217, 3.00GHz)

| SPECrate®2017_fp_base = 198 |
| SPECrate®2017_fp_peak = 202 |

| CPU2017 License: 55 | Test Sponsor: Dell Inc. | Test Date: Mar-2019 |
| Test Sponsor: Dell Inc. | Tested by: Dell Inc. | Hardware Availability: Apr-2019 |
| Tested by: Dell Inc. | | Software Availability: May-2019 |

**Peak Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++ (continued):
- `-qopt-mem-layout-trans=4`  
- `-auto -nostandard-realloc-lhs`  
- `-align array32byte`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links: