Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8260M, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 198</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak = Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (198)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>96</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>96</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>96</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>96</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>96</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>96</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>96</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>96</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>96</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>96</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Platinum 8260M</td>
</tr>
<tr>
<td>Max MHz: 3900</td>
</tr>
<tr>
<td>Nominal: 2400</td>
</tr>
<tr>
<td>Enabled: 96 cores, 4 chips</td>
</tr>
<tr>
<td>Orderable: 2,4 Chips</td>
</tr>
<tr>
<td>Cache L1: 32 KB I+32 KB D on chip per core</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3: 35.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage: 1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-25.28-default</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel: Yes</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4g released Jul-2019</td>
</tr>
<tr>
<td>File System: xfs</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Other: None</td>
</tr>
<tr>
<td>Power Management: --</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8260M, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>603.bwaves_s</td>
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<td>62.8</td>
<td>939</td>
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<td>939</td>
<td>62.8</td>
<td>939</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>96</td>
<td>74.3</td>
<td>224</td>
<td>74.3</td>
<td>224</td>
<td>74.3</td>
<td>224</td>
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<tr>
<td>619.lbm_s</td>
<td>96</td>
<td>34.4</td>
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<td>34.4</td>
<td>152</td>
<td>34.4</td>
<td>152</td>
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<tr>
<td>621.wrf_s</td>
<td>96</td>
<td>96.5</td>
<td>137</td>
<td>96.5</td>
<td>137</td>
<td>96.5</td>
<td>137</td>
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<tr>
<td>627.cam4_s</td>
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<td>160</td>
<td>55.3</td>
<td>160</td>
<td>55.3</td>
<td>160</td>
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<tr>
<td>628.pop2_s</td>
<td>96</td>
<td>187</td>
<td>63.5</td>
<td>187</td>
<td>63.5</td>
<td>187</td>
<td>63.5</td>
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<tr>
<td>638.imagick_s</td>
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<td>68.0</td>
<td>212</td>
<td>70.4</td>
<td>205</td>
<td>70.6</td>
<td>204</td>
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<tr>
<td>644.nab_s</td>
<td>96</td>
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<td>437</td>
<td>40.0</td>
<td>437</td>
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<td>436</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>96</td>
<td>102</td>
<td>89.4</td>
<td>103</td>
<td>88.1</td>
<td>107</td>
<td>85.5</td>
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<tr>
<td>654.roms_s</td>
<td>96</td>
<td>55.7</td>
<td>283</td>
<td>59.0</td>
<td>267</td>
<td>59.7</td>
<td>264</td>
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<tr>
<td>Peak</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 198
SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesysten page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8260M, 2.40GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017 Floating Point Speed Result</th>
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<td>Copyright 2017-2019 Standard Performance Evaluation Corporation</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base = 198**

**SPECspeed®2017_fp_peak = Not Run**

---

**Platform Notes**

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Disabled
- Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-09-21 295195f888a3d7edbe6e46a485a0011
running on linux-75co Fri Nov 22 04:32:01 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Platinum 8260M CPU @ 2.40GHz
- 4 "physical id"s (chips)
- 96 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores: 24
  - siblings: 24
  - physical 0: cores 0 1 2 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  - physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  - physical 2: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
  - physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 96
- On-line CPU(s) list: 0-95
- Thread(s) per core: 1
- Core(s) per socket: 24
- Socket(s): 4
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Platinum 8260M CPU @ 2.40GHz
- Stepping: 6
- CPU MHz: 2400.000
- CPU max MHz: 3900.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4800.00

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8260M, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_fp_base = 198
SPECspeed®2017_fp_peak = Not Run

Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
NUMA node2 CPU(s): 48-71
NUMA node3 CPU(s): 72-95

Flags: fpu vme de pse tsc msr pae mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmrperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrp pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_pinn ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512fd rdsuid adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsavesopt xsavec xgetbv1 xsavec qmmx_llc qmmx_occuseq qmmx_mtotal
qmmx_mbm_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni flush_l1d arch_capabilities

/proc/cpuinfo cache data
  cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physcial chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 385635 MB
node 0 free: 385307 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 387037 MB
node 1 free: 386884 MB
node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 2 size: 387067 MB
node 2 free: 386809 MB
node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 387065 MB
node 3 free: 382637 MB
node distances:
node 0 1 2 3
  0: 10 21 21 21
  1: 21 10 21 21
  2: 21 21 10 21
  3: 21 21 21 10

(Continued on next page)
Platform Notes (Continued)

From /proc/meminfo
MemTotal:       1583930088 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-75co 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Nov 22 02:17
SPEC is set to: /home/cpu2017
  Filesystem     Type  Size  Used Avail Use% Mounted on
  /dev/sda3      xfs   177G   72G  106G  41% /home

From /sys/devices/virtual/dmi/id
  BIOS:        Cisco Systems, Inc. C480M5.4.0.4g.0.0712190013 07/12/2019
  Vendor:      Cisco Systems Inc
  Product:     UCSC-C480-M5
  Serial:      FCH2223W00A

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
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SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Nov-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
-----------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

==============================================================================
Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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(Continued on next page)
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SPEC CPU®2017 Floating Point Speed Result
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Test Date: Nov-2019
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Software Availability: May-2019

Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

(Continued on next page)
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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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