Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6246, 3.30GHz)

SPECspeed®2017_int_base = 10.8
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

--- SPECspeed®2017_int_base (10.8) ---

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>48</td>
<td>25.0</td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>48</td>
<td>1.00</td>
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<tr>
<td>605.mcf_s</td>
<td>48</td>
<td>3.00</td>
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<tr>
<td>620.omnetpp_s</td>
<td>48</td>
<td>5.00</td>
<td></td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>48</td>
<td>7.00</td>
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<tr>
<td>625.x264_s</td>
<td>48</td>
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<tr>
<td>631.deepsjeng_s</td>
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<tr>
<td>641.leela_s</td>
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<td>13.0</td>
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<tr>
<td>648.exchange2_s</td>
<td>48</td>
<td>15.0</td>
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<tr>
<td>657.xz_s</td>
<td>48</td>
<td>17.0</td>
<td></td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 6246
Max MHz: 4200
Nominal: 3300
Enabled: 48 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I+ 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Desktop 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
          Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
**SPEC CPU®2017 Integer Speed Result**

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| Test Sponsor: | Cisco Systems |
| Test Date: | Dec-2019 |
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| Tested by: | Cisco Systems |
| Hardware Availability: | Apr-2019 |
| Software Availability: | May-2019 |

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>250</td>
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<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM

Memory using Red Hat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
 sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### SPEC CPU®2017 Integer Speed Result

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

#### Platform Notes

**BIOS Settings:**  
Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise

**SNC set to Disabled**  
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7ed6e6e6a485a0011  
running on linux-0enh Fri Dec 6 02:34:14 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo  
```plaintext
model name : Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
4 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
physical 0: cores 0 2 4 8 9 10 11 17 18 19 25 27
physical 1: cores 0 2 4 8 9 10 11 17 18 19 25 27
physical 2: cores 0 2 4 8 10 17 18 19 20 24 25 27
physical 3: cores 0 2 8 9 10 17 18 19 20 25 26 27
```

From lscpu:  
```plaintext
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
Stepping: 7
CPU MHz: 3300.000
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6600.00
```

(Continued on next page)
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Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-11
NUMA node1 CPU(s): 12-23
NUMA node2 CPU(s): 24-35
NUMA node3 CPU(s): 36-47
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cdp_l3 invpcid_single intel_pSTATE tpr_shadow vmmcall flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrm rdtscp mdin flushed dts reduction cmpxchg16b

/proc/cpuinfo cache data
cache size: 25344 KB
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 385468 MB
node 0 free: 385190 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 387059 MB
node 1 free: 386876 MB
node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35
node 2 size: 387059 MB
node 2 free: 386843 MB
node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47
node 3 size: 387027 MB
node 3 free: 386673 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

(Continued on next page)
# SPEC CPU®2017 Integer Speed Result

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## Platform Notes (Continued)

From `/proc/meminfo`

<table>
<thead>
<tr>
<th>MemTotal:</th>
<th>1583733472 kB</th>
</tr>
</thead>
<tbody>
<tr>
<td>HugePages_Total:</td>
<td>0</td>
</tr>
<tr>
<td>Hugepagesize:</td>
<td>2048 kB</td>
</tr>
</tbody>
</table>

From `/etc/*release*` /`/etc/*version*`

```
NAME="SLED"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
ID="sled"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sled:15"
```

```
uname -a:
Linux linux-0enh 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** No status reported
- **Microarchitectural Data Sampling:** No status reported
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Dec 6 02:28

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>224G</td>
<td>46G</td>
<td>178G</td>
<td>21%</td>
<td>/</td>
</tr>
</tbody>
</table>

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
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**Platform Notes (Continued)**

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

**Compiler Version Notes**

| C benchmarks: |
| icc -m64 -std=c11 |

| C++ benchmarks: |
| icpc -m64 |

| Fortran benchmarks: |
| ifort -m64 |

---

**Software Notes**

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**Compiler Invocation**

| C benchmarks: |
| icc -m64 -std=c11 |

| C++ benchmarks: |
| icpc -m64 |

| Fortran benchmarks: |
| ifort -m64 |
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### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
- 602.gcc_s: -DSPEC_LP64  
- 605.mcf_s: -DSPEC_LP64  
- 620.omnetpp_s: -DSPEC_LP64  
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX  
- 625.x264_s: -DSPEC_LP64  
- 631.deepsjeng_s: -DSPEC_LP64  
- 641.leela_s: -DSPEC_LP64  
- 648.exchange2_s: -DSPEC_LP64  
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**  
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
- L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**  
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- qopt-mem-layout-trans=4  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
- lqkmalloc

**Fortran benchmarks:**  
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
- nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:  

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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Originally published on 2019-12-24.