Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6252, 2.10GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base = 190</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>96</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>96</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>96</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>96</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>96</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>96</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>96</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>96</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>96</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>96</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Gold 6252
Max MHz: 3700
Nominal: 2100
Enabled: 96 cores, 4 chips
Orderable: 2.4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
Cache L2: 1 MB I+D on chip per core
Cache L3: 35.75 MB I+D on chip per core
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 960 GB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Desktop 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4i released Aug-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Dec-2019
Hardware Availability: Apr-2019
Software Availability: May-2019
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6252, 2.10GHz)

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SPEC CPU®2017 Floating Point Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECspeed®2017_fp_base = 190
SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Seconds</th>
<th>Seconds</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
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</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>96</td>
<td>71.4</td>
<td>826</td>
<td>65.7</td>
<td>898</td>
<td>64.5</td>
<td>915</td>
<td>190</td>
<td>212</td>
<td>190</td>
<td>212</td>
<td>190</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>96</td>
<td>78.8</td>
<td>212</td>
<td>78.7</td>
<td>212</td>
<td>78.5</td>
<td>212</td>
<td>190</td>
<td>212</td>
<td>190</td>
<td>212</td>
<td>190</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>96</td>
<td>77.1</td>
<td>67.9</td>
<td>48.9</td>
<td>107</td>
<td>34.9</td>
<td>150</td>
<td>190</td>
<td>107</td>
<td>190</td>
<td>107</td>
<td>190</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>96</td>
<td>101</td>
<td>131</td>
<td>100</td>
<td>132</td>
<td>100</td>
<td>132</td>
<td>190</td>
<td>132</td>
<td>190</td>
<td>132</td>
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</tr>
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<td>627.cam4_s</td>
<td>96</td>
<td>58.1</td>
<td>153</td>
<td>57.7</td>
<td>154</td>
<td>57.1</td>
<td>155</td>
<td>190</td>
<td>154</td>
<td>190</td>
<td>155</td>
<td>190</td>
</tr>
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<td>96</td>
<td>224</td>
<td>52.9</td>
<td>226</td>
<td>52.4</td>
<td>231</td>
<td>51.3</td>
<td>190</td>
<td>52.4</td>
<td>190</td>
<td>51.3</td>
<td>190</td>
</tr>
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<td>638.imagick_s</td>
<td>96</td>
<td>62.2</td>
<td>232</td>
<td>62.6</td>
<td>230</td>
<td>62.2</td>
<td>232</td>
<td>190</td>
<td>230</td>
<td>190</td>
<td>230</td>
<td>190</td>
</tr>
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<td>96</td>
<td>43.6</td>
<td>401</td>
<td>43.6</td>
<td>401</td>
<td>43.6</td>
<td>401</td>
<td>190</td>
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<td>190</td>
<td>401</td>
<td>190</td>
</tr>
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<td>96</td>
<td>84.6</td>
<td>108</td>
<td>86.1</td>
<td>106</td>
<td>85.0</td>
<td>107</td>
<td>190</td>
<td>106</td>
<td>190</td>
<td>107</td>
<td>190</td>
</tr>
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<td>288</td>
<td>54.8</td>
<td>287</td>
<td>53.4</td>
<td>295</td>
<td>190</td>
<td>287</td>
<td>190</td>
<td>295</td>
<td>190</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6252, 2.10GHz)

<table>
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<th>190</th>
</tr>
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<tbody>
<tr>
<td>SPECspeed®2017_fp_peak   =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  Test Date: Dec-2019
Test Sponsor: Cisco Systems  Hardware Availability: Apr-2019
Tested by: Cisco Systems  Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed81e64a46e485a0011
running on linux-3zzh Sun Dec 22 09:17:44 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
  4 "physical id"s (chips)  
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
CPU max MHz: 3700.0000
CPU min MHz: 1000.0000
BogoMIPS: 4200.00

(Continued on next page)
Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
NUMA node2 CPU(s): 48-71
NUMA node3 CPU(s): 72-95
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cdp_l3 invpcid_single intel_pppin mba tpr_shadow vmmx flexpriority ept vpid fsgsbase tsc_adjust bmis hle avx2 smep bmi2 ibrms invpcid rtm cmq mpx rdts a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cmq_llc cmq_occsp llc cmq_mbms total cmq_mbms local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
node 0 size: 385625 MB
node 0 free: 385034 MB
node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
node 1 size: 387056 MB
node 1 free: 386821 MB
node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 2 size: 387028 MB
node 2 free: 386776 MB
node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
node 3 size: 387054 MB
node 3 free: 386872 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

**Platform Notes (Continued)**

From /proc/meminfo
MemTotal: 1583887148 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
uname -a:
```
Linux linux-3zzh 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** No status reported  
- **Microarchitectural Data Sampling:** No status reported  
- **CVE-2017-5754 (Meltdown):** Not affected  
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization  
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW  

run-level 3 Dec 21 21:00

SPEC is set to: /home/cpu2017  
Filesystem Type Size Used Avail Use% Mounted on  
/dev/sda2 btrfs 893G 22G 871G 3% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C480M5.4.0.41.0.0831191123 08/31/2019  
Vendor: Cisco Systems Inc  
Product: UCSC-C480-M5  
Serial: FCH2243W038

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

*(Continued on next page)*
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6252, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Dec-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECspeed®2017_fp_base = 190
SPECspeed®2017_fp_peak = Not Run

Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C          | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Compiler Version Notes (Continued)

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
*******************************************************************************
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
*******************************************************************************

Compiler Version Notes (Continued)

==============================================================================
Fortran      | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
*******************************************************************************
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
*******************************************************************************

Compiler Version Notes (Continued)

==============================================================================
Fortran, C   | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
*******************************************************************************
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

(Continued on next page)
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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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