## SPEC CPU®2017 Integer Speed Result

<table>
<thead>
<tr>
<th>Application</th>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>64</td>
<td>7.96</td>
<td>9.68</td>
<td></td>
</tr>
<tr>
<td>gcc</td>
<td>64</td>
<td>10.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mcf</td>
<td>64</td>
<td>7.42</td>
<td>7.38</td>
<td></td>
</tr>
<tr>
<td>omnetpp</td>
<td>64</td>
<td>12.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>xalancbmk</td>
<td>64</td>
<td>12.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>x264</td>
<td>64</td>
<td>12.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>deepsjeng</td>
<td>64</td>
<td>5.47</td>
<td></td>
<td></td>
</tr>
<tr>
<td>leela</td>
<td>64</td>
<td>4.77</td>
<td></td>
<td></td>
</tr>
<tr>
<td>exchange2</td>
<td>64</td>
<td>16.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>xz</td>
<td>64</td>
<td>23.7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 6242
- **Max MHz:** 3900
- **Nominal:** 2800
- **Enabled:** 64 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

---

**Test Sponsor:** Cisco Systems  
**Test Date:** Dec-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>64</td>
<td>261</td>
<td>6.81</td>
<td>261</td>
<td>6.80</td>
<td>262</td>
<td>6.78</td>
<td>64</td>
<td>223</td>
<td>7.96</td>
<td>223</td>
<td>7.98</td>
<td>224</td>
<td>7.92</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>64</td>
<td>413</td>
<td>9.63</td>
<td>411</td>
<td>9.68</td>
<td>409</td>
<td>9.73</td>
<td>64</td>
<td>398</td>
<td>10.0</td>
<td>396</td>
<td>10.1</td>
<td>399</td>
<td>9.99</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>64</td>
<td>375</td>
<td>12.6</td>
<td>375</td>
<td>12.6</td>
<td>375</td>
<td>12.6</td>
<td>64</td>
<td>374</td>
<td>12.6</td>
<td>373</td>
<td>12.6</td>
<td>373</td>
<td>12.7</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>64</td>
<td>219</td>
<td>7.43</td>
<td>220</td>
<td>7.42</td>
<td>221</td>
<td>7.39</td>
<td>64</td>
<td>218</td>
<td>7.48</td>
<td>221</td>
<td>7.38</td>
<td>224</td>
<td>7.27</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>64</td>
<td>115</td>
<td>12.3</td>
<td>114</td>
<td>12.4</td>
<td>114</td>
<td>12.5</td>
<td>64</td>
<td>114</td>
<td>12.4</td>
<td>115</td>
<td>12.4</td>
<td>115</td>
<td>12.3</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>64</td>
<td>122</td>
<td>14.4</td>
<td>122</td>
<td>14.4</td>
<td>122</td>
<td>14.4</td>
<td>64</td>
<td>122</td>
<td>14.4</td>
<td>122</td>
<td>14.4</td>
<td>122</td>
<td>14.4</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>64</td>
<td>262</td>
<td>5.46</td>
<td>262</td>
<td>5.48</td>
<td>262</td>
<td>5.47</td>
<td>64</td>
<td>262</td>
<td>5.47</td>
<td>262</td>
<td>5.48</td>
<td>262</td>
<td>5.47</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>64</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
<td>4.78</td>
<td>357</td>
<td>4.78</td>
<td>64</td>
<td>358</td>
<td>4.77</td>
<td>357</td>
<td>4.77</td>
<td>357</td>
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</tr>
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<td>64</td>
<td>177</td>
<td>16.6</td>
<td>176</td>
<td>16.7</td>
<td>177</td>
<td>16.6</td>
<td>64</td>
<td>176</td>
<td>16.7</td>
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</tr>
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<td>261</td>
<td>23.7</td>
<td>261</td>
<td>23.7</td>
<td>64</td>
<td>260</td>
<td>23.8</td>
<td>260</td>
<td>23.8</td>
<td>260</td>
<td>23.8</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**
Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

<table>
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<th>SPECspeed®2017_int_peak</th>
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<tbody>
<tr>
<td>10.1</td>
<td>10.3</td>
</tr>
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</table>

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Test Date:** Dec-2019

**Hardware Availability:** Apr-2019

**Software Availability:** May-2019

### Platform Notes

**BIOS Settings:**
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise

**SNC set to Disabled**

**Patrol Scrub set to Disabled**

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on linux-icbf Sat Dec 14 23:56:40 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
  - 4 "physical id"s (chips)
  - 64 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 16
  - siblings : 16
  - physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  - physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 64
- On-line CPU(s) list: 0-63
- Thread(s) per core: 1
- Core(s) per socket: 16
- Socket(s): 4
- NUMA node(s): 4
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
- Stepping: 6
- CPU MHz: 2800.000
- CPU max MHz: 3900.0000
- CPU min MHz: 1200.0000
- BogoMIPS: 5600.00

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

SPECspeak\textsuperscript{\copyright}2017\textsubscript{\textregistered}\textsuperscript{\textregistered} \textsubscript{int\_base} = 10.1
SPECspeak\textsuperscript{\copyright}2017\textsubscript{\textregistered}\textsuperscript{\textregistered} \textsubscript{int\_peak} = 10.3

CPU2017 License: 9019
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Platform Notes (Continued)

- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 22528K
- NUMA node0 CPU(s): 0-15
- NUMA node1 CPU(s): 16-31
- NUMA node2 CPU(s): 32-47
- NUMA node3 CPU(s): 48-63
- Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpmr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_i3 cdp_l3 invpcid_single intel_ppa mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow invpcid rtm cqm mpx rdtp a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsavec1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

```
/proc/cpuinfo cache data
cache size: 22528 KB
```

(Continued on next page)
Platform Notes (Continued)

From /proc/meminfo
   MemTotal:       1583893712 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15"
      VERSION_ID="15"
      PRETTY_NAME="SUSE Linux Enterprise Server 15"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
   Linux linux-icbf 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):        No status reported
Microarchitectural Data Sampling:           No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Dec 14 23:54

SPEC is set to: /home/cpu2017
   Filesystem     Type   Size  Used Avail Use% Mounted on
   /dev/sdb2     trfs  222G  8.5G  213G   4% /home

From /sys/devices/virtual/dmi/id
   BIOS:    Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
   Vendor:  Cisco Systems, Inc.
   Product: UCSB-B480-M5
   Serial:  FLM230102QU

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

**CPU2017 License:** 9019
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**Tested by:** Cisco Systems

**Test Date:** Dec-2019
**Hardware Availability:** Apr-2019
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**Platform Notes (Continued)**

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

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**Compiler Version Notes**

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>---------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>C++</td>
<td>620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)</td>
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</tr>
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<td></td>
</tr>
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</tr>
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<td>---------</td>
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</tr>
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<td>Fortran</td>
<td>648.exchange2_s(base, peak)</td>
</tr>
<tr>
<td>---------</td>
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</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
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</tbody>
</table>
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**Base Compiler Invocation**

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

| SPECspeed®2017_int_base = 10.1 |
| SPECspeed®2017_int_peak = 10.3 |

CPU2017 License: 9019
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### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
- -L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- -l/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -ljkmalloc

**Fortran benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
- -nostandard-realloc-lhs

### Peak Compiler Invocation

**C benchmarks:**
- icc -m64 -std=c11

**C++ benchmarks:**
- icpc -m64

**Fortran benchmarks:**
- ifort -m64
## Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6242, 2.80GHz)

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</tr>
</tbody>
</table>

### Peak Portability Flags
Same as Base Portability Flags

### Peak Optimization Flags

**C benchmarks:**

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-\L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -\L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-\L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-\L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

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SPECspeed®2017_int_base = 10.1
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Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 623.xalancbmk_s
641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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