SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

<table>
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<td>526.blender_r</td>
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<td>527.cam4_r</td>
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<td>554.roms_r</td>
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</tbody>
</table>

**Hardware**

- **CPU Name**: redacted
- **Max MHz**: 0
- **Nominal**: 0
- **Enabled**: 0 cores, 1 chip, 0 threads/core

**Software**

- **OS**: SUSE Linux Enterprise Server 15 SP1
- **Compiler**: C/C++/Fortran: Version 2.0.0 of AOCC
- **Parallel**: No
Dell Inc.
PowerEdge R6515 (redacted)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrates®2017_fp_base =
SPECrates®2017_fp_peak =

**SPECrates®2017_fp_base =**
**SPECrates®2017_fp_peak =**

Test Date: Jan-2020
Hardware Availability: Apr-2020
Software Availability: Aug-2019

SPECrates has determined that this result does not comply with the SPECrates OSG Guidelines for General Availability and the SPECrates CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

### Hardware (Continued)

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<td>L3:</td>
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<td>Other:</td>
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<td>Memory:</td>
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### Software (Continued)

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<tr>
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<td>System State:</td>
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<tr>
<td>Peak Pointers:</td>
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<td>jemalloc: jemalloc memory allocator library v5.2.0</td>
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### Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.
<table>
<thead>
<tr>
<th>Dell Inc. PowerEdge R6515 (redacted)</th>
<th>Dell Inc.</th>
</tr>
</thead>
</table>

### SPEC CPU®2017 Floating Point Rate Result

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** Jan-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Aug-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

### Compiler Notes

The AMD64 AOCC Compiler Suite is available at  
http://developer.amd.com/amd-aocc/

### Submit Notes

The config file option 'submit' was used.  
'numactl' was used to bind copies to the cores.  
See the configuration file for details.

### Operating System Notes

- 'ulimit -s unlimited' was used to set environment stack size  
- 'ulimit -l 2097152' was used to set environment locked pages in memory limit  
- `runcpu` command invoked through `numactl` i.e.:  
  ```  
  numa 1 --interleave=all runcpu <etc>  
  ```  
- Set `dirty_ratio` to limit dirty cache to 8% of memory  
- Set `swappiness=1` to swap only if necessary  
- Set `zone_reclaim_mode=1` to free local node memory and avoid remote memory  
- Set `drop_caches=3` to reset caches before invoking `runcpu`  
- `dirty_ratio`, `swappiness`, `zone_reclaim_mode` and `drop_caches` were all set using privileged `echo` (e.g. `echo 1 > /proc/sys/vm/swappiness`).  
- Transparent huge pages set to 'always' for this run (OS default)

### Environment Variables Notes

Environment variables set by `runcpu` before the start of the run:  
`LD_LIBRARY_PATH = `/root/cpu2017-1.1.0/amd_rate_aocc200_rome_C_lib/64;/root/cpu2017-1.1.0/`  

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc. PowerEdge R6515 (redacted) SPECrate®2017_fp_base = SPECrate®2017_fp_peak =

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Jan-2020
Hardware Availability: Apr-2020
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Environment Variable Notes (Continued)

amd_rate_aocc200_rome_C_lib/32:
MALLOC_CONF = "retain:true"

General Notes

Binaries were compiled on a system with 2x AMD EPYC 7601 CPU + 512GB Memory using Fedora 26

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc: configured and built with GCC v9.1.0 in Ubuntu 19.04 with -O3 -znver2 -flto
jemalloc 5.2.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.2.0/jemalloc-5.2.0.tar.bz2

Platform Notes

BIOS settings:
NUMA Nodes Per Socket set to 4
CCX at NUMA Domain set to Enabled
System Profile set to Custom
CPU Power Management set to Maximum Performance
Memory Frequency set to Maximum Performance
Turbo Boost Enabled
Cstates set to Enabled
Memory Patrol Scrub Disabled
Memory Refresh Rate set to 1x
PCI ASPM L1 Link Power Management Disabled
Determinism Slider set to Power Determinism

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

Platform Notes (Continued)

Efficiency Optimized Mode Disabled
Memory Interleaving set to Disabled
Memory Freq set to 3200
Fan Speed = Maximum

Sysinfo program /root/cpu2017-1.1.0/bin/sysinfo
Rev: r6365 of 2019-08-21 5195f888a0d7edbe6e46a485a0011
running on linux-g3ob Sat 11 19:37:37 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
redacted

From lscpu
redacted

From /proc/cpuinfo: some data redacted

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
redacted

From /proc/meminfo
MemTotal: 131479104 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

Platform Notes (Continued)

uname -a:
    Linux linux-g3ob 4.12.14-1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5753 (Veloce): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5715 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5716 (Spectre variant 2): Mitigation: Full AMD retpoline, IBPB: conditional, IBRS_FW, STIBP: conditional, RSB filling

run-level 3 Nov 25 11:37 last=5

SPEC is set to: /root/cpu2017-1.1.0
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 440G 36G 405G 9% /

From /sys/devices/virtual/dmi/id
    BIOS: Dell Inc. 1.2.12 12/12/2019
    Vendor: Dell Inc.
    Product: PowerEdge R6515
    Product Family: PowerEdge

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

Platform Notes (Continued)

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
8x 80AD80B380AD HMA80GR7CJR8N-XN 16 GB 2 rank 3200
8x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 508.namd_r(base, peak) 510.parest_r(base, peak)
| 511.povray_r(base, peak) |
| 512.blender_r(base, peak) |
| 538.imagick_r(base, peak) |
| 544.nab_r(base, peak) |
==============================================================================
AOCC.LLVM.2.0.0.B191.2019_07_19 clang version 8.0.0 (CLANG: Jenkins
AOCC_2_0_0-Build# 91) (based on LLVM AOCC.LLVM.2.0.0.B191.2019_07_19)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /sppo/dev/compilers/aocc-compiler-2.0.0/bin

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
AOCC.LLVM.2.0.0.B191.2019_07_19 clang version 8.0.0 (CLANG: Jenkins
AOCC_2_0_0-Build#191) (based on LLVM AOCC.LLVM.2.0.0.B191.2019_07_19)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /sppo/dev/compilers/aocc-compiler-2.0.0/bin

==============================================================================
| C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
==============================================================================
(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Dell Inc.
PowerEdge R6515 (redacted)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

Compiler Version Notes (Continued)

C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)

(Continued on next page)
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

**Base Compiler Invocation**

C benchmarks:
clang

C++ benchmarks:
clang++

Fortran benchmarks:
flang

(Continued on next page)
Dell Inc.  
PowerEdge R6515 (redacted)  

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**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** Jan-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Aug-2019  

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

### Base Compiler Invocation (Continued)

- Benchmarks using both Fortran and C:
  - flang  
  - clang
- Benchmarks using both C and C++:
  - clang++  
  - clang
- Benchmarks using Fortran, C, and C++:
  - clang++  
  - clang  
  - flang

### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.ham_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_CASE_FLAG -Mbyteswapio -DSPEC_LP64
- 526.blender_r: -funsigned-char -D__BOOL_DEFINED -DSPEC_LP64
- 527.cam4_r: -DSPEC_CASE_FLAG -DSPEC_LP64
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

Base Optimization Flags

C benchmarks:
- `-flto -Wl,-mltv -Wl,-function-specialize`
- `-Wl,-mltv -Wl,-region-vectorize -Wl,-mltv -Wl,-vector-library=LIBMVEC`
- `-Wl,-mltv -Wl,-reduce-array-computations=3 -O3 -ffast-math`
- `-march=znver2 -fstruct-layout=3 -mltv -unroll-threshold=50`
- `-fremap-arrays -mltv -function-specialize -mltv -enable-gvn-hoist`
- `-mltv -reduce-array-computations=3 -mltv -global-vectorize-slp`
- `-mltv -vector-library=LIBMVEC -mltv -inline-threshold=1000`
- `-flv-function-specialization -z muldefs -lmvec -lamdlibm -ljemalloc -lflang`

C++ benchmarks:
- `-std=c++98 -flto -Wl,-mltv -Wl,-function-specialize`
- `-Wl,-mltv -Wl,-region-vectorize -Wl,-mltv -Wl,-vector-library=LIBMVEC`
- `-Wl,-mltv -Wl,-reduce-array-computations=3 -Wl,-mltv -reduce-array-computations=3 -mltv -unroll-threshold=100 -flv-function-specialization`
- `-mltv -enable-partial-unswitch -z muldefs -lmvec -lamdlibm -ljemalloc -lflang`

Fortran benchmarks:
- `-flto -Wl,-mltv -Wl,-function-specialize`
- `-Wl,-mltv -Wl,-region-vectorize -Wl,-mltv -Wl,-vector-library=LIBMVEC`
- `-Wl,-mltv -Wl,-reduce-array-computations=3 -O3 -March=znver2`
- `-funroll-loops -Mrecursive -mltv -vector-library=LIBMVEC -z muldefs`
- `-Kieee -fno-finite-math-only -lmvec -lamdlibm -ljemalloc -lflang`

Benchmarks using both Fortran and C:
- `-flto -Wl,-mltv -Wl,-function-specialize`
- `-Wl,-mltv -Wl,-region-vectorize -Wl,-mltv -Wl,-vector-library=LIBMVEC`
- `-Wl,-mltv -Wl,-reduce-array-computations=3 -O3 -ffast-math`
- `-march=znver2 -fstruct-layout=3 -mltv -unroll-threshold=50`
- `-fremap-arrays -mltv -function-specialize -mltv -enable-gvn-hoist`

(Continued on next page)
SPECCPU®2017 Floating Point Rate Result

Dell Inc.
PowerEdge R6515 (redacted)

SPECCPU®2017_fp_peak =
SPECCPU®2017_fp_base =

Dell Inc.
PowerEdge R6515 (redacted)

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-mlir -reduce-array-computations=3 -mlir -global-vectorize-slp
-mlir -vector-library=LIBMVEC -mlir -inline-threshold=1000
-flv-function-specialization -funroll-loops -Mrecursive -z muldefs
-Kieee -fno-finite-math-only -lmvec -lmdlibm -ljemalloc -lflang

Benchmarks using both C and C++:
-std=c++98 -flto -Wl,-mlir -function-specialize
-mlir -reduce-array-computations=3 -mlir -global-vectorize-slp
-mlir -vector-library=LIBMVEC -mlir -inline-threshold=1000
-flv-function-specialization -funroll-loops -Mrecursive -z muldefs
-Kieee -fno-finite-math-only -lmvec -lmdlibm -ljemalloc -lflang

Non-Compliant
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.
Dell Inc.  
PowerEdge R6515 (redacted)  

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<td>Dell Inc.</td>
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<td>Aug-2019</td>
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SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.

### Peak Compiler Invocation

<table>
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<tr>
<th>C benchmarks:</th>
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<tr>
<td>C++ benchmarks:</td>
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<tr>
<td>Benchmarks using Fortran, C, and C++:</td>
<td>clang++ clang flang</td>
</tr>
</tbody>
</table>

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:

- 519.lbm_r: basepeak = yes
- 538.imagick_r: basepeak = yes

(Continued on next page)
Dell Inc.  
PowerEdge R6515 (redacted)  

<table>
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**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** Jan-2020  
**Hardware Availability:** Apr-2020  
**Software Availability:** Aug-2019

**Peak Optimization Flags (Continued)**

```
544.nab_r: -flto -Wl,-mllvm -Wl,-function-specialize
-W1,-mllvm -W1,-region-vectorize
-W1,-mllvm -W1,-vector-library=LIBMVEC
-W1,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver2 -mno-sse4a -fstruct-layout=5
-mllvm --vectorize-memory-aggressively
-mllvm --function-specialize,mllvm --enable-gvn-hoist
-mllvm -unroll-threshold=50 -mvec
-mllvm --vector-library=LIBMVEC
-mllvm --reduce-array-computations=3
-mllvm --global-vectorize-lp
-mllvm --inline-threshold=1000
-flv-function-specialization
-lmvec
-lamdlibm
-ljemalloc
-lflang
```

**C++ benchmarks:**

- 508.namd_r: basepeak = yes
- 510.parest_r: basepeak = yes

**Fortran benchmarks:**

- 503.bwaves_r: basepeak = yes
- 549.fotonik3d_r: basepeak = yes
- 554.roms_r: basepeak = yes

**Benchmarks using both Fortran and C:**

- 521.wrf_r: basepeak = yes
- 527.cam4_r: -flto -Wl,-mllvm -W1,-function-specialize -W1,-mllvm -W1,-region-vectorize

---

**Non-Compliant**

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.
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Peak Optimization Flags (Continued)

527.cam4_r (continued):
-Wl,-mllvm -Wl,-vector-library=LIBMVEC
-Wl,-mllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver2 -mno-sse4a -fstruct-layout=5
-mllvm -vectorize-memory-aggressively
-mllvm -function-specialize -mllvm -enable-gvn-hoist
-mllvm -unroll-threshold=50 -fremap-arrays
-mllvm -vector-library=LIBMVEC
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp -mllvm -inline-threshold=1000
-flv-function-specialization -O3 -funroll-loops
-Mrecursive -Klee -m infinite-math-only -lmvec
-lamdlibm -ljemalloc -lflang

Benchmarks using both C and C++:
511.povray_r: -std=c++11 -ftlo -Wl,-mllvm -Wl,-function-specialize
-Wl,-mllvm -Wl,-region-vectorize
-Wl,-mllvm -Wl,-vector-library=LIBMVEC
-Wl,-mllvm -Wl,-reduce-array-computations=3
-Wl,-mllvm -Wl,-x86-use-vzeroupper=false -Ofast
-march=znver2 -mno-sse4a -fstruct-layout=5
-mllvm -vectorize-memory-aggressively
-mllvm -function-specialize -mllvm -enable-gvn-hoist
-mllvm -unroll-threshold=50 -fremap-arrays
-mllvm -vector-library=LIBMVEC
-mllvm -reduce-array-computations=3
-mllvm -global-vectorize-slp -mllvm -inline-threshold=1000
-flv-function-specialization -mllvm -unroll-threshold=100
-mllvm -enable-partial-unswitch
-mllvm -loop-unswitch-threshold=200000 -lmvec -lamdlibm
-ljemalloc -lflang

(Continued on next page)
### Dell Inc. PowerEdge R6515 (redacted)

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<td>Software Availability: Aug-2019</td>
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**SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, at this time, the submitter is not able to make a public statement of intent to ship this particular configuration.**

**Peak Optimization Flags (Continued)**

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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