## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 5218, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>166</td>
<td>167</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Jan-2020

**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2019

**Tested by:** Cisco Systems  
**Software Availability:** May-2019

### Threads

<table>
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<th>hw</th>
<th>64</th>
<th>4</th>
<th>9</th>
<th>14</th>
<th>19</th>
<th>24</th>
</tr>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
<td>126</td>
<td>114</td>
<td>110</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
<td>126</td>
<td>114</td>
<td>110</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
<td>126</td>
<td>114</td>
<td>110</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
<td>126</td>
<td>114</td>
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<td>126</td>
<td>114</td>
<td>110</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
<td>126</td>
<td>114</td>
<td>110</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
<td>126</td>
<td>114</td>
<td>110</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>64</td>
<td>166</td>
<td>150</td>
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<td>110</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
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<td>150</td>
<td>126</td>
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<td>150</td>
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<td>110</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Gold 5218  
- **Max MHz:** 3900
- **Nominal:** 2300
- **Enabled:** 64 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Threads</th>
<th>Base Seconds</th>
<th>Base Ratio</th>
<th>Peak Threads</th>
<th>Peak Seconds</th>
<th>Peak Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>64 66.7 885</td>
<td>66.9 882 66.2</td>
<td>891</td>
<td>64 66.5 887</td>
<td>66.3 890</td>
<td>66.7 885</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>64 100 167</td>
<td>101 166 101 165</td>
<td>64 101 165</td>
<td>100 166</td>
<td>100 166</td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>64 36.5 144</td>
<td>35.7 147 35.9</td>
<td>146</td>
<td>64 34.1 154</td>
<td>34.9 150</td>
<td>38.5 136</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>64 105 126</td>
<td>104 127 105 126</td>
<td>64 105 126</td>
<td>105 126</td>
<td>105 126</td>
<td></td>
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<td>77.8 114 77.9</td>
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<td>76.9 115</td>
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</tr>
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<td>64 249 47.7</td>
<td>261 45.5 254</td>
<td>46.7</td>
<td>64 243 48.8</td>
<td>247 48.1</td>
<td>249 47.7</td>
</tr>
<tr>
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<td>64 85.9 168</td>
<td>84.9 170 86.2</td>
<td>167</td>
<td>64 87.7 164</td>
<td>85.0 170</td>
<td>89.9 161</td>
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<tr>
<td>644.nab_s</td>
<td>64 59.1 296</td>
<td>58.8 297 58.9</td>
<td>297</td>
<td>64 58.8 297</td>
<td>58.7 298</td>
<td>58.8 297</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>64 82.0 111</td>
<td>83.7 109 81.8</td>
<td>111</td>
<td>64 82.7 110</td>
<td>82.9 110</td>
<td>83.7 109</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>64 77.7 203</td>
<td>75.7 208 78.3</td>
<td>201</td>
<td>64 76.2 207</td>
<td>78.0 202</td>
<td>77.4 203</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

---

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
 sync; echo 3 > /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPECspeed®2017_fp_base = 166
SPECspeed®2017_fp_peak = 167

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jan-2020
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e646a485a0011
running on linux-icbf Mon Jan 20 10:35:45 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name: Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
4 "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 16
siblings: 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
Stepping: 6
CPU MHz: 2300.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 4600.00
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 5218, 2.30GHz)

| SPECspeed®2017_fp_base = 166 |
| SPECspeed®2017_fp_peak = 167 |

Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
NUMA node2 CPU(s): 32-47
NUMA node3 CPU(s): 48-63
Flags: fpu vme de pse tsc msr pae mce sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdp_13 invpcid_single intel_p impoverished tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ersed invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xsavec xsaveopt xgetbv1 xsaves cqm_llc cqm_occupy_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
  cache size : 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  node 0 size: 385627 MB
  node 0 free: 385291 MB
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
  node 1 size: 387058 MB
  node 1 free: 379862 MB
  node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 2 size: 387058 MB
  node 2 free: 386558 MB
  node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
  node 3 size: 387026 MB
  node 3 free: 386789 MB
  node distances:
    node 0 1 2 3
    0: 10 21 31 21
    1: 21 10 21 31
    2: 31 21 10 21
    3: 21 31 21 10

From /proc/meminfo

(Continued on next page)
## Platform Notes (Continued)

- **MemTotal:** 1583893680 kB
- **HugePages_Total:** 0
- **Hugepagesize:** 2048 kB

```
From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-icbf 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux
```

### Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** No status reported
- **Microarchitectural Data Sampling:** No status reported
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

```
run-level 3 Jan 20 05:54
```

- **SPEC is set to:** /home/cpu2017
- **Filesystem** | **Type** | **Size** | **Used** | **Avail** | **Use%** | **Mounted on**
  - /dev/sdb2  | btrfs  | 222G  | 15G  | 207G  | 7%  | /home

```
From /sys/devices/virtual/dmi/id
  BIOS:  Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
  Vendor:  Cisco Systems Inc
  Product:  UCSB-B480-M5
  Serial:  FLM230102QU
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

### Memory:
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPEC\textregistered2017 fp\_base = 166
SPEC\textregistered2017 fp\_peak = 167

Platform Notes (Continued)

48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

<table>
<thead>
<tr>
<th>Platform</th>
<th>Program</th>
<th>SPECspeed\textregistered2017 fp_base</th>
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SPECSpeed®2017_fp_base = 166
SPECSpeed®2017_fp_peak = 167

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Compiler Version Notes (Continued)
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags
603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp

(Continued on next page)
## Base Optimization Flags (Continued)

Fortran benchmarks (continued):

```
-nostandard-realloc-lhs
```

Benchmarks using both Fortran and C:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
```

Benchmarks using Fortran, C, and C++:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Peak Portability Flags

Same as Base Portability Flags

## Peak Optimization Flags

C benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
```

Fortran benchmarks:
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- **Tested by:** Cisco Systems
- **Test Date:** Jan-2020
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019

### Peak Optimization Flags (Continued)

#### 603.bwaves_s

- `-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP`
- `-DSPEC_OPENMP -o2 -xCORE-AVX512 -qopt-prefetch -ipo -O3`
- `ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4`
- `-qopenmp -nostandard-realloc-lhs`

#### 649.fotonik3d_s

- `Same as 603.bwaves_s`

#### 654.roms_s

- `-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4`
- `-qopenmp -nostandard-realloc-lhs`

### Benchmarks using both Fortran and C:

#### 621.wrf_s

- `-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512`
- `-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div`
- `-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp`
- `-DSPEC_OPENMP -nostandard-realloc-lhs`

#### 627.cam4_s

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
- `-DSPEC_OPENMP -nostandard-realloc-lhs`

#### 628.pop2_s

- `Same as 621.wrf_s`

### Benchmarks using Fortran, C, and C++:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
- `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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