# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>284</td>
<td>330</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>292</td>
<td>340</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>192</td>
<td>331</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>192</td>
<td>367</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>271</td>
<td>405</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>256</td>
<td>404</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>256</td>
<td>649</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>235</td>
<td>678</td>
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<tr>
<td>548.exchange2_r</td>
<td>207</td>
<td>662</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>207</td>
<td>664</td>
</tr>
</tbody>
</table>

## Hardware

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Platinum 8268</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz:</td>
<td>3900</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2900</td>
</tr>
<tr>
<td>Enabled:</td>
<td>48 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>35.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 1.9 TB SSD SAS</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

## Software

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.4c released Apr-2019</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management:</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPEC CPU®2017 Integer Rate Result

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SPECrate®2017_int_base = 315
SPECrate®2017_int_peak = 330

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>500.perlbench_r</td>
<td>96</td>
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<td>554</td>
<td>246</td>
<td>551</td>
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<td>96</td>
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<td>256</td>
<td>611</td>
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<td>624</td>
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<td>499</td>
<td>208</td>
<td>501</td>
<td>207</td>
<td>500</td>
<td>207</td>
</tr>
</tbody>
</table>

SPECrate®2017_int_base = 315
SPECrate®2017_int_peak = 330

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numacltl i.e.:
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

**SPEC CPU®2017 Integer Rate Result**

**SPECrate®2017_int_base = 315**

**SPECrate®2017_int_peak = 330**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Jan-2020</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
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</tbody>
</table>

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**General Notes (Continued)**

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbbe6e464885a0011
running on linux-4z0x Fri Jan 24 15:47:28 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8268 CPU @ 2.90GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

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### Platform Notes (Continued)

- **Socket(s):** 2
- **NUMA node(s):** 4
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Platinum 8268 CPU @ 2.90GHz
- **Stepping:** 6
- **CPU MHz:** 2900.000
- **CPU max MHz:** 3900.0000
- **CPU min MHz:** 1200.0000
- **BogoMIPS:** 5800.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 36608K
- **NUMA node0 CPU(s):** 0-3,7-9,13-15,19,20,48-51,55-57,61-63,67,68
- **NUMA node1 CPU(s):** 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
- **NUMA node2 CPU(s):** 24-27,31-33,37-39,43,44,72-75,79-81,85-87,91,92
- **NUMA node3 CPU(s):** 28-30,34-36,40-42,45-47,76-78,82-84,88-90,93-95

**Flags:**
- fpu
- vme
- de
- pse
- tsc
- msr
- pae
- mce
- cx8
- apic
- sep
- mtrr
- pge
- mca
- cmov
- pat
- pse36
- clflush
- dts
- acpi
- mmx
- fxsr
- sse
- sse2
- ss
- ht
- tm
- pbe
- syscall
- nx
- pdpe1gb
- rdtscp
- lahf
- lm
- constant_tsc
- art
- arch_perfmon
- pebs
- bts
- rep_good
- nopl
- xtopology
- nonstop_tsc
- cpuid
- svm
- ept
- svmcmp
- eptvd
- fmmu_delays
- nonlsync_ept
- svmcheck

**/proc/cpuinfo cache data**
- **cache size:** 36608 KB

From numactl --hardware

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

- **available:** 4 nodes (0-3)
  - node 0 cpus: 0 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68
  - node 0 size: 192101 MB
  - node 0 free: 191665 MB
  - node 1 cpus: 4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71
  - node 1 size: 193497 MB
  - node 1 free: 193247 MB
  - node 2 cpus: 24 25 26 27 31 32 33 37 38 39 43 44 72 73 74 75 79 80 81 85 86 87 91 92
  - node 2 size: 193526 MB

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**SPEC CPU®2017_int_base = 315**

**SPEC CPU®2017_int_peak = 330**

**CPU2017 License:** 9019

**Test Sponsor:** Cisco Systems

**Test Date:** Jan-2020

**Hardware Availability:** Apr-2019

**Tested by:** Cisco Systems

**Software Availability:** May-2019
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECrate®2017_int_base = 315
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CPU2017 License: 9019
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Tested by: Cisco Systems

Platform Notes (Continued)

node 2 free: 193198 MB
node 3 cpus: 28 29 30 34 35 40 41 42 45 46 47 76 77 78 82 83 84 88 89 90 93 94 95
node 3 size: 193523 MB
node 3 free: 193245 MB
node distances:
node 0 1 2 3
  0:  10  11 21 21
  1:  11  10 21 21
  2:  21  21 10 11
  3:  21  21 11 10

From /proc/meminfo
MemTotal:       791191776 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jan 24 08:23

SPEC is set to: /home/cpu2017

Filesystem  Type  Size  Used Avail Use% Mounted on
/dev/sdaf1   xfs  891G  52G  839G   6% /

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECrater®2017_int_base = 315
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C240M5.4.0.4c.0.0411190411 04/11/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP21460G08

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502 gcc_r (peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 500 perlbench_r base, peak 502 gcc_r base 505 mcf_r base, peak
| 525 x264_r base, peak 557 xz_r base, peak
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 502 gcc_r (peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
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==============================================================================

==============================================================================
C       | 500 perlbench_r base, peak 502 gcc_r base 505 mcf_r base, peak
| 525 x264_r base, peak 557 xz_r base, peak
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPEC CPU®2017 Integer Rate Result
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SPECratenode2017_int_base = 315
SPECratenode2017_int_peak = 330

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Jan-2020
Tested by: Cisco Systems
Hardware Availability: Apr-2019
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Compiler Version Notes (Continued)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
      531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
      531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

 SPECrate\textsuperscript{\textregistered}2017\textunderscore int\textunderscore peak = 330
SPECrate\textsuperscript{\textregistered}2017\textunderscore int\textunderscore base = 315

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64
502.gcc\_r: -DSPEC\_LP64
505.mcf\_r: -DSPEC\_LP64
520.omnetpp\_r: -DSPEC\_LP64
523.xalancbmk\_r: -DSPEC\_LP64 -DSPEC\_LINUX
525.x264\_r: -DSPEC\_LP64
531.deepsjeng\_r: -DSPEC\_LP64
541.leela\_r: -DSPEC\_LP64
548.exchange2\_r: -DSPEC\_LP64
557.xz\_r: -DSPEC\_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lgkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lgkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lgkmalloc
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Software Availability: May-2019

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11

$02.gcc_r:icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
icpc -m64

$23.xalancbmk_r:icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64  -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64  -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1)  -prof-use(pass 2)  -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -1jemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4

(Continued on next page)
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CPU2017 License: 9019
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Software Availability: May-2019

Peak Optimization Flags (Continued)

505.mcf_r (continued):
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r -W1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml
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Cisco UCS C240 M5 (Intel Xeon Platinum 8268, 2.90GHz)

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<th>Test Date: Jan-2020</th>
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<td>Software Availability: May-2019</td>
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-01-24 05:17:27-0500.
Report generated on 2020-02-18 18:05:44 by CPU2017 PDF formatter v6255.
Originally published on 2020-02-18.