SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.70 GHz, Intel Xeon Gold 6258R)

SPECrate®2017_fp_base = 269
SPECrate®2017_fp_peak = Not Run

Test Sponsor: HPE
Tested by: HPE
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Test Date: Jan-2020

503.bwaves_r 112
507.cactuBSSN_r 112
508.namd_r 112
510.parest_r 112
511.povray_r 112
519.lbm_r 112
521.wrf_r 112
526.blender_r 112
527.cam4_r 112
538.imagick_r 112
544.nab_r 112
549.fotonik3d_r 112
554.roms_r 112

Hardware

CPU Name: Intel Xeon Gold 6258R
Max MHz: 4000
Nominal: 2700
Enabled: 56 cores, 2 chips, 2 threads/core
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 38.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)
Storage: 1 x 400 GB SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)
Kernel 4.12.14-195-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler Build 20190416 for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler Build 20190416 for Linux
Parallel: No
Firmware: HPE BIOS Version I42 2.30 (12/10/2019) released Feb-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage
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<tr>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>112</td>
<td>2128</td>
<td>528</td>
<td>2125</td>
<td>528</td>
<td>2129</td>
<td>527</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>112</td>
<td>581</td>
<td>244</td>
<td>582</td>
<td>243</td>
<td>581</td>
<td>244</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>112</td>
<td>416</td>
<td>255</td>
<td>416</td>
<td>256</td>
<td>417</td>
<td>255</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>112</td>
<td>2256</td>
<td>130</td>
<td>2258</td>
<td>130</td>
<td>2266</td>
<td>129</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>112</td>
<td>703</td>
<td>372</td>
<td>701</td>
<td>373</td>
<td>704</td>
<td>371</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>112</td>
<td>910</td>
<td>130</td>
<td>910</td>
<td>130</td>
<td>909</td>
<td>130</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>112</td>
<td>1088</td>
<td>230</td>
<td>1085</td>
<td>231</td>
<td>1089</td>
<td>230</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>112</td>
<td>547</td>
<td>312</td>
<td>547</td>
<td>312</td>
<td>547</td>
<td>312</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>112</td>
<td>550</td>
<td>356</td>
<td>548</td>
<td>357</td>
<td>549</td>
<td>357</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>112</td>
<td>365</td>
<td>763</td>
<td>364</td>
<td>766</td>
<td>364</td>
<td>765</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>112</td>
<td>345</td>
<td>547</td>
<td>345</td>
<td>547</td>
<td>344</td>
<td>548</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>112</td>
<td>2545</td>
<td>172</td>
<td>2543</td>
<td>172</td>
<td>2543</td>
<td>172</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>112</td>
<td>1777</td>
<td>100</td>
<td>1787</td>
<td>99.6</td>
<td>1780</td>
<td>100</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:  
```
numactl --interleave=all runcpu <etc>
```

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:  
```
LD_LIBRARY_PATH = "$
```
General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed81e6a46a485a0011
running on sy480-sles15sp1-hs Sun Jan 26 12:26:58 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6258R CPU @ 2.70GHz
  2 "physical id"s (chips)
  112 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 28
  siblings : 56
  physical 0: cores 0 1 2 3 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29
    30
  physical 1: cores 0 1 2 3 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29
    30

From lscpu:

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE
Test Date: Jan-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 112
On-line CPU(s) list: 0-111
Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6258R CPU @ 2.70GHz
Stepping: 7
CPU MHz: 2700.000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-13, 56-69
NUMA node1 CPU(s): 14-27, 70-83
NUMA node2 CPU(s): 28-41, 84-97
NUMA node3 CPU(s): 42-55, 98-111
Flags:

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 56 57 58 59 60 61 62 63 64 65 66 67 68 69
node 0 size: 96285 MB

(Continued on next page)
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<td>Jun-2019</td>
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</table>

Test Sponsor: HPE
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes (Continued)

node 0 free: 95848 MB
node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80 81 82 83
node 1 size: 96733 MB
node 1 free: 96464 MB
node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 84 85 86 87 88 89 90 91 92 93 94 95 96 97
node 2 size: 96762 MB
node 2 free: 96486 MB
node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105 106 107 108 109 110 111
node 3 size: 96580 MB
node 3 free: 96083 MB
node distances:
  node 0 1 2 3
  0: 10 21 21 21
  1: 21 10 21 21
  2: 21 21 10 21
  3: 21 21 21 10

From /proc/meminfo
MemTotal: 395633728 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
  NAME=’SLES’
  VERSION=’15-SP1’
  VERSION_ID=’15.1’
  PRETTY_NAME=’SUSE Linux Enterprise Server 15 SP1’
  ID=’sles’
  ID_LIKE=’suse’
  ANSI_COLOR=’0;32’
  CPE_NAME=’cpe:/o:suse:sles:15:sp1’

uname –a:
Linux sy480-sles15sp1-hs 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019
(8fba516) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp

(Continued on next page)
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Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):
Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):
Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jan 26 12:26

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda4 xfs 143G 31G 113G 22% /home

From /sys/devices/virtual/dmi/id
BIOS: HPE I42 12/10/2019
Vendor: HPE
Product: Synergy 480 Gen10
Product Family: Synergy
Serial: MXQ72204FC

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SM BIOS* standard.
Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++             | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base)
(Continued on next page)

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**Compiler Version Notes (Continued)**

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

**Base Compiler Invocation**

C benchmarks:
```bash
icc -m64 -std=c11
```
## Base Compiler Invocation (Continued)

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

Benchmarks using both Fortran and C:
```bash
ifort -m64 icc -m64 -std=c11
```

Benchmarks using both C and C++:
```bash
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
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<td>503.bwaves_r</td>
<td>-DSPEC_LP64</td>
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<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX -funsigned-char</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>-DSPEC_LP64 -DSPEC_CASE_FLAG</td>
</tr>
<tr>
<td>538.imagick_r</td>
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<tr>
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<td>554.roms_r</td>
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</tr>
</tbody>
</table>

## Base Optimization Flags

### C benchmarks:
```bash
-xCORE-AVX512 -ipo -03 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4
```

### C++ benchmarks:
```bash
-xCORE-AVX512 -ipo -03 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4
```
Hewlett Packard Enterprise  
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Base Optimization Flags (Continued)

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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