## SPEC CPU®2017 Integer Speed Result

**Tyrone Systems**

(Test Sponsor: Netweb Pte Ltd)

**DIT400TR-48RL**

(2.50 GHz, Intel Xeon Gold 6248)

**SPECspeed®2017_int_base = 10.2**

**SPECspeed®2017_int_peak = 10.4**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
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<tr>
<td>perlbench_s</td>
<td>80</td>
<td>6.86</td>
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<tr>
<td>gcc_s</td>
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<td>9.84</td>
<td>10.2</td>
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<td>mcf_s</td>
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<td>omnetpp_s</td>
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<tr>
<td>xalancbmk_s</td>
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<td>12.4</td>
<td>12.4</td>
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<tr>
<td>x264_s</td>
<td>80</td>
<td>14.4</td>
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<tr>
<td>deepsjeng_s</td>
<td>80</td>
<td>5.45</td>
<td>5.45</td>
</tr>
<tr>
<td>leela_s</td>
<td>80</td>
<td>4.75</td>
<td>4.75</td>
</tr>
<tr>
<td>exchange2_s</td>
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<td>16.1</td>
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<tr>
<td>xz_s</td>
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<td>23.7</td>
<td>24.1</td>
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</table>

**CPU2017 License:** 006042

**Test Sponsor:** Netweb Pte Ltd

**Test Date:** Feb-2020

**Hardware Availability:** Sep-2019

**Tested by:** Netweb

**Software Availability:** Aug-2019

### Hardware

- **CPU Name:** Intel Xeon Gold 6248
- **Max MHz:** 3900
- **Nominal:** 2500
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1, 2 (chip)s
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 27.5 MB I+D on chip per chip
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
- **Storage:** 1 x 480 GB SSD
- **Other:** None

### Software

- **OS:** CentOS Linux release 7.7.1908 (Core) 3.10.0-1062.el7.x86_64
- **Compiler:** C/C++: Version 19.0.4.243 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.243 of Intel Fortran Compiler Build 20190416 for Linux
- **Parallel:** Yes
- **Firmware:** Version V8.101 released Aug-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** Default
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SPECCPU 2017 Integer Speed Result

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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>24.1</td>
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</tbody>
</table>

SPECspeed 2017_int_base = 10.2
SPECspeed 2017_int_peak = 10.4

Compiler Notes

SPEC has learned that this result, which used an evaluation compiler, was submitted contrary to the compiler license terms.
Intel has granted a one-time waiver for this result.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
DIT400TR-48RL
(2.50 GHz, Intel Xeon Gold 6248)

SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Netweb

General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f88a3d7eddb1e6e46a485a0011
running on NODE8 Thu Feb  6 09:54:24 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
 2 "physical id"s (chips)
 80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                80
On-line CPU(s) list:   0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz

(Continued on next page)
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CPU MHz: 999.908
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19,40-59
NUMA node1 CPU(s): 20-39,60-79

Flags: fpu vme de pse tsc msr pae mce cmovpat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx vfpv10 f16c rdrnd lahf_lm abm 3nowprefetch epb cat_l3 cdp_l3 intel_pinnings inter-pm sbb ibrs ibsp ibrs-enhanced tpr_shadow vmx.flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb avx512bw avx512vl xsaveopt xsaveprec xgetbv1 cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts hwp hwp_act_window hwp-epp hwp_pkg_req pku ospke avx512_vnni md_clear spec_ctrl intel_stibp flush_l1d arch_capabilities

/platformuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

Available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
node 0 size: 195228 MB
node 0 free: 163667 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
node 1 size: 196608 MB
node 1 free: 167186 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo

MemTotal: 394857620 kB
HugePages_Total: 0

(Continued on next page)
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Tested by: Netweb

Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*:
  centos-release: CentOS Linux release 7.7.1908 (Core)
  centos-release-upstream: Derived from Red Hat Enterprise Linux 7.7 (Source)
  os-release:
    NAME="CentOS Linux"
    VERSION="7 (Core)"
    ID="centos"
    ID_LIKE="rhel fedora"
    VERSION_ID="7"
    PRETTY_NAME="CentOS Linux 7 (Core)"
    ANSI_COLOR="0;31"
    CPE_NAME="cpe:/o:centos:centos:7"
  redhat-release: CentOS Linux release 7.7.1908 (Core)
  system-release: CentOS Linux release 7.7.1908 (Core)
  system-release-cpe: cpe:/o:centos:centos:7

uname -a:
  Linux NODE8 3.10.0-1062.10.2.el7.x86_64 #1 SMP Wed Aug 7 18:08:02 UTC 2019 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences, __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Full retpoline, IBPB

run-level 3 Feb 4 18:18

SPEC is set to: /home/cpu2017

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/mapper/centos-home</td>
<td>xfs</td>
<td>392G</td>
<td>122G</td>
<td>271G</td>
<td>31%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id:
  BIOS: American Megatrends Inc. V8.101 08/02/2019
  Vendor: Tyrone Systems
  Product: DIT400TR-48RL
  Serial: empty

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow
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CPU2017 License: 006042  Test Date: Feb-2020
Test Sponsor: Netweb Pte Ltd  Hardware Availability: Sep-2019
Tested by: Netweb  Software Availability: Aug-2019

Platform Notes (Continued)

hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C   | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak) |
==============================================================================
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| icc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC. |
==============================================================================

==============================================================================
| C++ | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) |
| 631.deepsjeng_s(base, peak) 641.leela_s(base, peak) |
==============================================================================
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| icpc: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC. |
==============================================================================

==============================================================================
| Fortran | 648.exchange2_s(base, peak) |
==============================================================================
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.243 Build 20190416 |
| Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| ifort: NOTE: The evaluation period for this product ends on 2-nov-2019 UTC. |
==============================================================================

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
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SPECspeed®2017_int_peak = 10.4

CPU2017 License: 006042
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**Base Compiler Invocation (Continued)**

Fortran benchmarks:

ifort -m64

---

**Base Portability Flags**

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

---

**Base Optimization Flags**

C benchmarks:
-W1, -z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1, -z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

---

**Peak Compiler Invocation**

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
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<td>= 10.4</td>
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</table>

CPU2017 License: 006042  
Test Sponsor: Netweb Pte Ltd  
Tested by: Netweb  
Test Date: Feb-2020  
Hardware Availability: Sep-2019  
Software Availability: Aug-2019

### Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl, -z, multidefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp  
-DSPEC_OPENMP -fno-strict-overflow  
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl, -z, multidefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3  
-no-prec-div -DSPEC_SUPPRESS_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl, -z, multidefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4  
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl, -z, multidefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl, -z, multidefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4

*(Continued on next page)*
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(2.50 GHz, Intel Xeon Gold 6248)

<table>
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<th>CPU2017 License: 006042</th>
<th>SPECspeed®2017_int_base = 10.2</th>
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<td>Test Sponsor: Netweb Pte Ltd</td>
<td>SPECspeed®2017_int_peak = 10.4</td>
</tr>
<tr>
<td>Tested by: Netweb</td>
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</tr>
</tbody>
</table>

**Peak Optimization Flags (Continued)**

620.omnetpp_s (continued):
-DSPEC_SUPPRESS_OPENMP  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64 -lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.243/linux/compiler/lib/intel64 -lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/TyroneIT-Platform-Settings-V1-CLX-revA.html  

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/TyroneIT-Platform-Settings-V1-CLX-revA.xml  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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