Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

<table>
<thead>
<tr>
<th>SPEC CPU®2017 Integer Rate Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
</tr>
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<td>Test Date: Feb-2020</td>
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<th>SPECrate®2017_int_base = 306</th>
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<tr>
<td>SPECrate®2017_int_peak = 320</td>
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**Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)**

<table>
<thead>
<tr>
<th>Copies</th>
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<tr>
<td>500.perlbench_r 112</td>
<td>274</td>
<td>258</td>
</tr>
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<td>502.gcc_r 112</td>
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<td>505.mcf_r 112</td>
<td>382</td>
<td>381</td>
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<td>520.omnetpp_r 112</td>
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<td>523.xalancbmk_r 112</td>
<td>638</td>
<td>667</td>
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<td>525.x264_r 112</td>
<td>634</td>
<td>655</td>
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<td>257</td>
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</tr>
<tr>
<td>557.xz_r 112</td>
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</tr>
</tbody>
</table>

**Hardware**

- **CPU Name**: Intel Xeon Gold 6238R
- **Max MHz**: 4000
- **Nominal**: 2200
- **Enabled**: 56 cores, 2 chips, 2 threads/core
- **Orderable**: 1.2 Chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **L2**: 1 MB I+D on chip per core
- **L3**: 38.5 MB I+D on chip per chip
- **Other**: None
- **Memory**: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage**: 1 x 960 GB SSD SAS
- **Other**: None

**Software**

- **OS**: SUSE Linux Enterprise Server 15 (x86_64)
  4.12.14-25.25-default
- **Compiler**: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel**: No
- **Firmware**: Version 4.0.4j released Aug-2019
- **File System**: xfs
- **System State**: Run level 5 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: 32/64-bit
- **Other**: jemalloc memory allocator V5.0.1
- **Power Management**: BIOS set to prefer performance at the cost of additional power usage
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

**SPECrated®2017_int_base = 306**

**SPECrated®2017_int_peak = 320**

<table>
<thead>
<tr>
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<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
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<td>238</td>
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<td>502.gcc_r</td>
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<td>505.mcf_r</td>
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<td><strong>257</strong></td>
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<td><strong>586</strong></td>
<td><strong>206</strong></td>
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<td>206</td>
<td>586</td>
<td>206</td>
<td>112</td>
<td>586</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)  

General Notes (Continued)

numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1b6e64a485a0011
running on linux-17bx Wed Feb 26 17:52:27 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6238R CPU @ 2.20GHz
  2 "physical id"s (chips)
  112 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 56
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lsmpcpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 112
On-line CPU(s) list: 0-111

(Continued on next page)
Cisco Systems
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SPEC CPU®2017 Integer Rate Result

SPECrate®2017_int_base = 306
SPECrate®2017_int_peak = 320

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Thread(s) per core: 2
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6238R CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2200.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-3,7-9,14-17,21-23,56-59,63-65,70-73,77-79
NUMA node1 CPU(s): 4-6,10-13,18-20,24-27,60-62,66-69,74-76,80-83
NUMA node2 CPU(s): 28-31,35-37,42-45,49-51,84-87,91-93,98-101,105-107
NUMA node3 CPU(s): 32-34,38-41,46-48,52-55,58-90,94-97,102-104,108-111

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 cflflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3

From numactl --hardware
Available: 4 nodes (0-3)
Node 0 cpus: 0 1 2 3 7 8 9 14 15 16 17 21 22 23 56 57 58 59 63 64 65 70 71 72 73 77 78 79
Node 0 size: 192034 MB
Node 0 free: 191471 MB
Node 1 cpus: 4 5 6 10 11 12 13 18 19 20 24 25 26 27 60 61 62 66 67 68 69 74 75 76 80 81 82 83

(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

SPEC CPU®2017 Integer Rate Result
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Platform Notes (Continued)

node 1 size: 193530 MB
node 1 free: 193174 MB
node 2 cpus: 28 29 30 31 35 36 37 42 43 44 45 49 50 51 84 85 86 87 91 92 93 98 99 100
101 105 106 107
node 2 size: 193501 MB
node 2 free: 192749 MB
node 3 cpus: 32 33 34 38 39 40 41 46 47 48 52 53 54 55 88 89 90 94 95 96 97 102 103 104
108 109 110 111
node 3 size: 193319 MB
node 3 free: 192919 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 790922752 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
o-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID=sles
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

(Continued on next page)
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Platform Notes (Continued)

run-level 5 Feb 26 17:50
SPEC is set to: /home/cpu2017
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   324G   44G  280G  14% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP223909MB

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
         | 525.x264_r(base, peak) 557.xz_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C       | 502.gcc_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416

(Continued on next page)
## Compiler Version Notes (Continued)

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---

C
| 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak) 

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 523.xalancbmk_r(peak) 

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) 

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 523.xalancbmk_r(peak) 

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) 

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

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SPECrater®2017_int_peak = 320

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Compiler Version Notes (Continued)

Fortran | 548.exchange2_r (base, peak)
------------------------------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

(Continued on next page)
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

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- 9019

### Test Sponsor
- Cisco Systems

### Tested by
- Cisco Systems

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<td>Feb-2020</td>
<td>Feb-2020</td>
<td>May-2019</td>
</tr>
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</table>

### Base Optimization Flags (Continued)

- **C++ benchmarks (continued):**
  - `-qopt-mem-layout-trans=4`
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
  - `-lqkmalloc`

- **Fortran benchmarks:**
  - `-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
  - `-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte`
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`
  - `-lqkmalloc`

### Peak Compiler Invocation

**Peak Compiler Invocation**

- **C benchmarks (except as noted below):**
  - `icc -m64 -std=c11`

- **502.gcc_r:**
  - `icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin`

- **C++ benchmarks (except as noted below):**
  - `icpc -m64`

- **523.xalancbmk_r:**
  - `icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin`

- **Fortran benchmarks:**
  - `ifort -m64`

### Peak Portability Flags

- **500.perlbench_r:**
  - `-DSPEC_LP64 -DSPEC_LINUX_X64`

- **502.gcc_r:**
  - `-D_FILE_OFFSET_BITS=64`

- **505.mcf_r:**
  - `-DSPEC_LP64`

- **520.omnetpp_r:**
  - `-DSPEC_LP64`

- **523.xalancbmk_r:**
  - `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`

- **525.x264_r:**
  - `-DSPEC_LP64`

- **531.deepsjeng_r:**
  - `-DSPEC_LP64`

- **541.leela_r:**
  - `-DSPEC_LP64`

- **548.exchange2_r:**
  - `-DSPEC_LP64`

- **557.xz_r:**
  - `-DSPEC_LP64`
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)  

| SPECrate®2017_int_base | 306 |
| SPECrate®2017_int_peak | 320 |

**Peak Optimization Flags**

**C benchmarks:**

```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r
```

**C++ benchmarks:**

```
520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -03 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r
```

**Fortran benchmarks:**

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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**CPU2017 License**: 9019  
**Test Sponsor**: Cisco Systems  
**Tested by**: Cisco Systems  
**Test Date**: Feb-2020  
**Hardware Availability**: Feb-2020  
**Software Availability**: May-2019

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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