Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Copies

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
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<td>113</td>
</tr>
<tr>
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<td>48</td>
<td>113</td>
<td>113</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>48</td>
<td>109</td>
<td>109</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>48</td>
<td>83.1</td>
<td>83.0</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>48</td>
<td>167</td>
<td>188</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>48</td>
<td>92.2</td>
<td>92.2</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>48</td>
<td>157</td>
<td>162</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>48</td>
<td>142</td>
<td>143</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>48</td>
<td>157</td>
<td>161</td>
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<td>48</td>
<td></td>
<td>322</td>
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<tr>
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<td>48</td>
<td></td>
<td>233</td>
</tr>
<tr>
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<td>48</td>
<td>123</td>
<td>123</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>48</td>
<td>71.3</td>
<td>71.5</td>
</tr>
</tbody>
</table>

Hardware
CPU Name: Intel Xeon Silver 4214R
Max MHz: 3500
Nominal: 2400
Enabled: 24 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 16.5 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
Storage: 1 x 960 GB SSD SAS
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4j released Aug-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)  

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Results Table

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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
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<tr>
<td>503.bwaves_r</td>
<td>48</td>
<td>1237</td>
<td>389</td>
<td>1238</td>
<td>389</td>
<td>1239</td>
<td>389</td>
<td>1238</td>
<td>389</td>
<td>1239</td>
<td>389</td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>48</td>
<td>541</td>
<td>112</td>
<td>540</td>
<td>113</td>
<td>540</td>
<td>113</td>
<td>540</td>
<td>113</td>
<td></td>
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<td></td>
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</tr>
<tr>
<td>508.namd_r</td>
<td>48</td>
<td>417</td>
<td>109</td>
<td>419</td>
<td>109</td>
<td>417</td>
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<td>417</td>
<td>109</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>48</td>
<td>1509</td>
<td>83.2</td>
<td>1514</td>
<td>82.9</td>
<td>1510</td>
<td>83.1</td>
<td>1514</td>
<td>82.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>48</td>
<td>671</td>
<td>167</td>
<td>670</td>
<td>167</td>
<td>664</td>
<td>169</td>
<td>670</td>
<td>167</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>549</td>
<td>92.2</td>
<td>548</td>
<td>92.3</td>
<td>549</td>
<td>92.2</td>
<td>549</td>
<td>92.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>48</td>
<td>686</td>
<td>157</td>
<td>673</td>
<td>160</td>
<td>685</td>
<td>157</td>
<td>686</td>
<td>157</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td>48</td>
<td>513</td>
<td>142</td>
<td>512</td>
<td>143</td>
<td>513</td>
<td>142</td>
<td>513</td>
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<td>533</td>
<td>157</td>
<td>528</td>
<td>159</td>
<td>545</td>
<td>154</td>
<td>529</td>
<td>159</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>48</td>
<td>370</td>
<td>322</td>
<td>370</td>
<td>323</td>
<td>371</td>
<td>322</td>
<td>370</td>
<td>323</td>
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<td></td>
<td></td>
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<td>233</td>
<td>346</td>
<td>234</td>
<td>350</td>
<td>231</td>
<td>347</td>
<td>233</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td>48</td>
<td>1519</td>
<td>123</td>
<td>1519</td>
<td>123</td>
<td>1520</td>
<td>123</td>
<td>1520</td>
<td>123</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>48</td>
<td>1069</td>
<td>71.3</td>
<td>1071</td>
<td>71.2</td>
<td>1070</td>
<td>71.3</td>
<td>1067</td>
<td>71.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

| SPECrate®2017_fp_base = 146 |
| SPECrate®2017_fp_peak = 149 |

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |

| Test Date: | Feb-2020 |
| Hardware Availability: | Feb-2020 |
| Software Availability: | May-2019 |

**General Notes (Continued)**

```plaintext
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
```

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb1e6e46a485a0011
running on linux-4z0x Thu Feb 27 11:32:59 2020

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
  2 "physical id"s (chips)
  48 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 12
    siblings : 24
    physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
    physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
```

From lscpu:
```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
```

(Continued on next page)
## Platform Notes (Continued)

- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
- **Stepping:** 7
- **CPU MHz:** 2400.000
- **CPU max MHz:** 3500.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 4800.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 16896K

**NUMA node0 CPU(s):** 0-2, 6-8, 24-26, 30-32
**NUMA node1 CPU(s):** 3-5, 9-11, 27-29, 33-35
**NUMA node2 CPU(s):** 12-14, 18-20, 36-38, 42-44
**NUMA node3 CPU(s):** 15-17, 21-23, 39-41, 45-47

**Flags:**
- fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdelgb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebp cat_13 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware

- WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 4 nodes (0-3)
  - node 0 cpus: 0 1 2 6 7 8 24 25 26 30 31 32
  - node 0 size: 192104 MB
  - node 0 free: 183167 MB
  - node 1 cpus: 3 4 5 9 10 11 27 28 29 33 34 35
  - node 1 size: 193499 MB
  - node 1 free: 188018 MB
  - node 2 cpus: 12 13 14 18 19 20 36 37 38 42 43 44
  - node 2 size: 193528 MB
  - node 2 free: 188037 MB
  - node 3 cpus: 15 16 17 21 22 23 39 40 41 45 46 47
  - node 3 size: 193526 MB

(Continued on next page)
### Platform Notes (Continued)

Node 3 free: 187914 MB

Node distances:
- Node 0: 10 11 21 21
- Node 1: 11 10 21 21
- Node 2: 21 21 10 11
- Node 3: 21 21 11 10

From /proc/meminfo:
- MemTotal: 791203052 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*:
```bash
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"
```

```bash
uname -a:
  Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:
- CVE-2018-3620 (L1 Terminal Fault): No status reported
- Microarchitectural Data Sampling: No status reported
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 27 03:09

SPEC is set to: /home/cpu2017

```bash
Filesystem  Type  Size   Used  Avail Use% Mounted on
/dev/sdaf1  xfs  891G  73G   818G   9%  /
```

From /sys/devices/virtual/dmi/id:
```bash
BIOS:  Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
```
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 146
SPECrate®2017_fp_peak = 149

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP21460GO8

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
==============================================================================

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

SPECrater®2017_fp_base = 146
SPECrater®2017_fp_peak = 149

CPU2017 License: 9019
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Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                | 554.roms_r(base, peak)
------------------------------------------------------------------------------

------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
------------------------------------------------------------------------------

------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Cisco Systems  
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)  
SPECrates\textsuperscript{\textregistered}2017\textsubscript{fp}_peak = 149  
SPECrates\textsuperscript{\textregistered}2017\textsubscript{fp}_base = 146

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Feb-2020  
Hardware Availability: Feb-2020  
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### Base Compiler Invocation (Continued)

Benchmarks using both C and C++:

icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:

icpc -m64 icc -m64 -std=c11 ifort -m64

### Base Portability Flags

- 503.bwaves_r: -DSPEC\_LP64
- 507.cactuBSSN_r: -DSPEC\_LP64
- 508.namd_r: -DSPEC\_LP64
- 510.parest_r: -DSPEC\_LP64
- 511.povray_r: -DSPEC\_LP64
- 519.lbm_r: -DSPEC\_LP64
- 521.wrf_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big_endian
- 526.blender_r: -DSPEC\_LP64 -DSPEC\_Linux -funsigned-char
- 527.cam4_r: -DSPEC\_LP64 -DSPEC\_CASE\_FLAG
- 538.imagick_r: -DSPEC\_LP64
- 544.nab_r: -DSPEC\_LP64
- 549.fotonik3d_r: -DSPEC\_LP64
- 554.roms_r: -DSPEC\_LP64

### Base Optimization Flags

#### C benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

#### C++ benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

#### Fortran benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

#### Benchmarks using both Fortran and C:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz) SPECrate®2017_fp_base = 146
SPECrate®2017_fp_peak = 149

CPU2017 License: 9019
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Test Date: Feb-2020
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Base Optimization Flags (Continued)

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

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SPECrate®2017_fp_peak = 149

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Test Sponsor: Cisco Systems
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Peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)
**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Silver 4214R, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 146</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 149</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

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**Peak Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++ (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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