## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

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<tr>
<th>Test Sponsor</th>
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<th>CPU2017 License</th>
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<tbody>
<tr>
<td>Cisco Systems</td>
<td>Feb-2020</td>
<td>9019</td>
<td>Cisco Systems</td>
<td>May-2019</td>
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</tbody>
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### SPECspeed®2017_int_base = 10.6

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_peak = 10.8</th>
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### Threads

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
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<tbody>
<tr>
<td>perlbench_s</td>
<td>56</td>
<td>8.12</td>
<td>10.8</td>
</tr>
<tr>
<td>gcc_s</td>
<td>56</td>
<td>10.4</td>
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<td>mcf_s</td>
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<td>9.42</td>
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<tr>
<td>omnetpp_s</td>
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<td>9.69</td>
<td></td>
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<td>xalancbmk_s</td>
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<td>12.6</td>
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<td>x264_s</td>
<td>56</td>
<td>14.7</td>
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<tr>
<td>deepsjeng_s</td>
<td>56</td>
<td>5.60</td>
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<tr>
<td>leela_s</td>
<td>56</td>
<td>4.89</td>
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<tr>
<td>exchange2_s</td>
<td>56</td>
<td>17.0</td>
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<tr>
<td>xz_s</td>
<td>56</td>
<td>24.2</td>
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### Software

- OS: SUSE Linux Enterprise Server 15 (x86_64)
- Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- Parallel: Yes
- Firmware: Version 4.0.4j released Aug-2019
- File System: xfs
- System State: Run level 5 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Other: jemalloc memory allocator V5.0.1
- Power Management: BIOS set to prefer performance at the cost of additional power usage

### Hardware

- CPU Name: Intel Xeon Gold 6238R
- Max MHz: 4000
- Nominal: 2200
- Enabled: 56 cores, 2 chips
- Orderable: 1.2 Chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 38.5 MB I+D on chip per chip
- Other: None
- Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- Storage: 1 x 960 GB SSD SAS
- Other: None

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Results Table

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<tr>
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<td>254</td>
<td>24.3</td>
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Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
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Cisco UCS C240 M5 (Intel Xeon Gold 6238R, 2.20GHz)

SPECspeed®2017_int_base = 10.6
SPECspeed®2017_int_peak = 10.8

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Disabled
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a001
running on linux-17bx Fri Feb 28 19:17:15 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6238R CPU @ 2.20GHz
  2 "physical id"s (chips)
  56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27
28 29 30

From 1scpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6238R CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2200.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x

(Continued on next page)
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**Platform Notes (Continued)**

- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 39424K
- NUMA node0 CPU(s): 0-27
- NUMA node1 CPU(s): 28-55
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
  lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
  xtrn pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
  avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
  invpcid_single intel_pni ssbd mba ibrs ibpb stibp tpr_shadow vnmi flexpriority ept
  vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rd_extensions_a
  avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
  xsaveopt xax64 xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
  dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni
  flush_l1d arch_capabilities

```
/proc/cpuinfo cache data
cache size : 39424 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

```bash
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 0 size: 385541 MB
node 0 free: 384355 MB
node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52
node 1 size: 386855 MB
node 1 free: 386314 MB
node distances:
  node 0 1
  0: 10 21
  1: 21 10
```

From /proc/meminfo
```
MemTotal: 790934376 KB
HugePages_Total: 0
Hugepagesize: 2048 KB
```

From /etc/*release* /etc/*version*
```
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
```

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Platform Notes (Continued)

PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: ___user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 5 Feb 28 19:16

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda3 xfs 324G 44G 280G 14% /home

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
    Vendor: Cisco Systems Inc
    Product: UCSC-C240-M5L
    Serial: WZP223909MB

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
        24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

    (End of data from sysinfo program)

Compiler Version Notes
==============================================================================
| C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) |
(Continued on next page)
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Compiler Version Notes (Continued)

| peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
-----------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++     | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
| 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 648.exchange2_s(base, peak)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64

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### Base Portability Flags (Continued)

- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
  -L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

**Fortran benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
  -nostandard-realloc-lhs

### Peak Compiler Invocation

**C benchmarks:**
- icc -m64 -std=c11

**C++ benchmarks:**
- icpc -m64

**Fortran benchmarks:**
- ifort -m64

### Peak Portability Flags

Same as Base Portability Flags
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Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass l) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass l) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass l) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass l) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass l) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

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<tbody>
<tr>
<td>10.6</td>
<td>10.8</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Peak Optimization Flags (Continued)
Fortran benchmarks (continued):
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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