Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPECrater®2017_int_base = 282
SPECrater®2017_int_peak = 294

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4j released Aug-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage

Hardware
CPU Name: Intel Xeon Gold 6242R
Max MHz: 4100
Nominal: 3100
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 35.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 960 GB SSD SAS
Other: None

Tests
500.perlbench_r 80
502.gcc_r 80
505.mcf_r 80
520.omnetpp_r 80
523.xalancbmk_r 80
525.x264_r 80
531.deepsjeng_r 80
541.leela_r 80
548.exchange2_r 80
557.xz_r 80

500.perlbench_r
502.gcc_r
505.mcf_r
520.omnetpp_r
523.xalanchbmk_r
525.x264_r
531.deepsjeng_r
541.leela_r
548.exchange2_r
557.xz_r

SPECrater®2017_int_base (282)
SPECrater®2017_int_peak (294)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 282
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Results Table

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</tr>
</tbody>
</table>

SPECrate®2017_int_base = 282
SPECrate®2017_int_peak = 294

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPECrate®2017_int_base = 282
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<td>Feb-2020</td>
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<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbbie6e46a485a0011
running on linux-4z0x Mon Feb 24 03:12:28 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 5 6 10 11 12 13 16 17 18 19 21 24 26 27 28 29
physical 1: cores 0 1 2 3 5 6 9 10 12 13 16 17 18 19 20 21 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per core: 20

(Continued on next page)
Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
Stepping: 7
CPU MHz: 3100.000
CPU max MHz: 4100.0000
CPU min MHz: 1200.0000
BogoMIPS: 6200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,6,10-12,15,16,40-43,46,50-52,55,56
NUMA node1 CPU(s): 4,5,7-9,13,14,17-19,44,45,47-49,53,54,57-59
NUMA node2 CPU(s): 20-23,26,27,30-32,36,60-63,66,67,70-72,76
NUMA node3 CPU(s): 24,25,28,29,33-35,37-39,64,65,68,69,73-75,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdeldstmt dts rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref perf_tsc msr pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdeldstmt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_t13 cdv_l3 invpcid_single intel_pinn mba tpr_shadow vmx flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmq mpx rdtsve
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsave xsaveopt xgetbv xsaveopt xsaves xsaveopt xgetbv xsaveopt xgetbv

/proc/cpuinfo cache data
   cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 6 10 11 12 15 16 40 41 42 43 46 50 51 52 55 56
   node 0 size: 192102 MB
   node 0 free: 191732 MB
   node 1 cpus: 4 5 7 8 9 13 14 17 18 19 44 45 47 48 49 53 54 57 58 59
   node 1 size: 193526 MB
   node 1 free: 193253 MB
   node 2 cpus: 20 21 22 23 26 27 30 31 32 36 60 61 62 63 66 67 70 71 72 76
   node 2 size: 193526 MB

(Continued on next page)
Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPECrace\textsuperscript{®}2017\textsuperscript{®}\textsuperscript{®} int\_base = 282
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Platform Notes (Continued)

node 2 free: 193288 MB
node 3 cpus: 24 25 28 29 33 34 35 37 38 39 64 65 68 69 73 74 75 77 78 79
node 3 size: 193496 MB
node 3 free: 193115 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791196896 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-4z0x 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS\_FW

run-level 3 Feb 24 03:08

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdh1 xfs 891G 51G 841G 6% /
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

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CPU2017 License: 9019  Test Date: Feb-2020
Test Sponsor: Cisco Systems  Hardware Availability: Feb-2020
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Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP21460GO8

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

<table>
<thead>
<tr>
<th>C</th>
<th>502.gcc_r(peak)</th>
</tr>
</thead>
<tbody>
<tr>
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 523.xalancbmk_r(peak)
---

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
---

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 523.xalancbmk_r(peak)
---

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
    | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
---

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

Fortran | 548.exchange2_r(base, peak)
---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Cisco Systems
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Software Availability: May-2019

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
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Peak Compiler Invocation

C benchmarks (except as noted below):
  icc -m64 -std=c11
  502.gcc_r.icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
  icpc -m64
  523.xalancbmk_r.icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
  ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
  500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
  -fno-strict-overflow
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc
  502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
  -L/usr/local/je5.0.1-32/lib -ljemalloc
  505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

| SPECrate®2017_int_base = 282 |
| SPECrate®2017_int_peak = 294 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Optimization Flags (Continued)

505.mcf_r (continued):
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6242R, 3.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 282</th>
<th>SPECrate®2017_int_peak = 294</th>
</tr>
</thead>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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