## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>79.4</td>
<td>79.9</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Hardware

- **CPU Name:** Intel Xeon Silver 4215R  
- **Max MHz:** 4000  
- **Nominal:** 3200  
- **Enabled:** 16 cores, 2 chips  
- **Orderable:** 1.2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 11 MB I+D on chip per core  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
- **Storage:** 1 x 960 GB SSD SAS  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.4j released Aug-2019  
- **File System:** xfs  
- **System State:** Run level 5 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Baseline</th>
<th>Ratio</th>
<th>Median Baseline</th>
<th>Ratio</th>
<th>Peak</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>16</td>
<td>186</td>
<td>318</td>
<td>186</td>
<td>317</td>
<td>186</td>
<td>317</td>
</tr>
<tr>
<td>607.cactubssn_s</td>
<td>16</td>
<td>193</td>
<td>86.6</td>
<td>194</td>
<td>86.1</td>
<td>193</td>
<td>86.4</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>16</td>
<td>77.2</td>
<td>67.9</td>
<td>77.6</td>
<td>67.5</td>
<td>77.0</td>
<td>68.0</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>16</td>
<td>161</td>
<td>82.3</td>
<td>162</td>
<td>81.5</td>
<td>163</td>
<td>81.3</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>16</td>
<td>215</td>
<td>41.3</td>
<td>213</td>
<td>41.6</td>
<td>213</td>
<td>41.6</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>16</td>
<td>231</td>
<td>51.4</td>
<td>229</td>
<td>51.8</td>
<td>230</td>
<td>51.7</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>16</td>
<td>238</td>
<td>60.6</td>
<td>238</td>
<td>60.6</td>
<td>239</td>
<td>60.5</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>16</td>
<td>149</td>
<td>117</td>
<td>149</td>
<td>117</td>
<td>149</td>
<td>117</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>16</td>
<td>153</td>
<td>59.5</td>
<td>150</td>
<td>60.8</td>
<td>150</td>
<td>60.8</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>16</td>
<td>222</td>
<td>70.8</td>
<td>223</td>
<td>70.5</td>
<td>220</td>
<td>71.5</td>
</tr>
</tbody>
</table>

---

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "'/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_fp_base = 79.4
SPECspeed®2017_fp_peak = 79.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2020
Hardware Availability: Feb-2020
Tested by: Cisco Systems
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7e5b1e6e485a0011
running on linux-l7bx Mon Feb 24 22:29:22 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 8
  siblings : 8
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 16
  On-line CPU(s) list: 0-15
  Thread(s) per core: 1
  Core(s) per socket: 8
  Socket(s): 2
  NUMA node(s): 2
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
  Stepping: 7
  CPU MHz: 3200.000
  CPU max MHz: 4000.0000
  CPU min MHz: 1000.0000
  BogoMIPS: 6400.00
  Virtualization: VT-x
  L1d cache: 32K
  L1i cache: 32K
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPEC®2017_fp_base = 79.4
SPEC®2017_fp_peak = 79.9

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abtm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_pmm ssbd mba ibrs ibpb stibp tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsave xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local
dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni
flush_l1d arch_capabilities

From /proc/cpuinfo cache data
  cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 385574 MB
  node 0 free: 383379 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 386830 MB
  node 1 free: 380391 MB
  node distances:
  node 0 1
  0: 10 21
  1: 21 10

From /proc/meminfo
  MemTotal: 790942576 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_fp_base = 79.4
SPECspeed®2017_fp_peak = 79.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBFB, IBRS_FW

run-level 5 Feb 24 17:33

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda3 xfs 324G 50G 274G 16% /home

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
    Vendor: Cisco Systems Inc
    Product: UCSC-C240-M5L
    Serial: WZP223909MB

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)                      |
| 644.nab_s(base, peak) |
==============================================================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)  

SPEC®2017_fp_base = 79.4
SPEC®2017_fp_peak = 79.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                | 654.roms_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                | 628.pop2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Base Compiler Invocation

C benchmarks:
   icc -m64 -std=c11

Fortran benchmarks:
   ifort -m64

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.2GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

**SPEC Specification**

**SPEC CPU®2017 Floating Point Speed Result**

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>79.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>79.9</td>
</tr>
</tbody>
</table>

**Base Compiler Invocation (Continued)**

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

**Base Portability Flags**

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_fp_base = 79.4
SPECspeed®2017_fp_peak = 79.9

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2020
Hardware Availability: Feb-2020
Tested by: Cisco Systems
Software Availability: May-2019

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_fp_base = 79.4
SPECspeed®2017_fp_peak = 79.9

Peak Optimization Flags (Continued)

627.cam4_s: \texttt{-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs}

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
\texttt{-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs}

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-02-25 01:29:21-0500.
Report generated on 2020-03-17 16:20:26 by CPU2017 PDF formatter v6255.
Originally published on 2020-03-17.