# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Software Availability:</th>
<th>Feb-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64)</td>
<td>4.12.14-23-default</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
<td></td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.4j released Aug-2019</td>
<td></td>
</tr>
<tr>
<td>File System:</td>
<td>btrfs</td>
<td></td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>32/64-bit</td>
<td></td>
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<tr>
<td>Other:</td>
<td>jemalloc memory allocator V5.0.1</td>
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<tr>
<td>Power Management:</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
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</tbody>
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<table>
<thead>
<tr>
<th>Hardware</th>
<th>Hardware Availability:</th>
<th>May-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Bronze 3206R</td>
<td></td>
</tr>
<tr>
<td>Max MHz:</td>
<td>1900</td>
<td></td>
</tr>
<tr>
<td>Nominal:</td>
<td>1900</td>
<td></td>
</tr>
<tr>
<td>Enabled:</td>
<td>16 cores, 2 chips</td>
<td></td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 Chips</td>
<td></td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
<td></td>
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<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
<td></td>
</tr>
<tr>
<td>L3:</td>
<td>11 MB I+D on chip per chip</td>
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<tr>
<td>Other:</td>
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<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)</td>
<td></td>
</tr>
<tr>
<td>Storage:</td>
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<tr>
<td>Other:</td>
<td>None</td>
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</table>

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base = 55.0</th>
<th>SPECrate®2017_int_peak = 56.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>16</td>
<td>50.1</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>16</td>
<td>55.7</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>16</td>
<td>66.2</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>16</td>
<td>40.7</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>16</td>
<td>66.4</td>
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<tr>
<td>525.x264_r</td>
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<tr>
<td>531.deepsjeng_r</td>
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<td>43.4</td>
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<tr>
<td>541.leela_r</td>
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<td>36.0</td>
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<tr>
<td>548.exchange2_r</td>
<td>16</td>
<td>109</td>
</tr>
<tr>
<td>557.xz_r</td>
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<td>114</td>
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</table>

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Tested by:** Cisco Systems
**Test Date:** Feb-2020
**Hardware Availability:** Feb-2020
**Software Availability:** May-2019
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>44.6</td>
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<td>50.7</td>
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<tr>
<td>505.mcf_r</td>
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<td>390</td>
<td>66.3</td>
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<td>66.2</td>
<td>391</td>
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<td>520.omnetpp_r</td>
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<td>36.0</td>
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<td>36.1</td>
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<td>16</td>
<td>367</td>
<td>114</td>
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<td>365</td>
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<td>16</td>
<td>367</td>
<td>114</td>
<td>366</td>
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<tr>
<td>557.xz_r</td>
<td>16</td>
<td>541</td>
<td>31.9</td>
<td>541</td>
<td>32.0</td>
<td>541</td>
<td>31.9</td>
<td>16</td>
<td>541</td>
<td>32.0</td>
<td>541</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th><strong>CPU2017 License:</strong></th>
<th>9019</th>
</tr>
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<tbody>
<tr>
<td><strong>Test Sponsor:</strong></td>
<td>Cisco Systems</td>
</tr>
<tr>
<td><strong>Tested by:</strong></td>
<td>Cisco Systems</td>
</tr>
<tr>
<td><strong>Test Date:</strong></td>
<td>Feb-2020</td>
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<tr>
<td><strong>Hardware Availability:</strong></td>
<td>Feb-2020</td>
</tr>
<tr>
<td><strong>Software Availability:</strong></td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base = 55.0**
**SPECrate®2017_int_peak = 56.1**

## General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


## Platform Notes

**BIOS Settings:**
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019–08–21 295195f888a3d7edbbe6e46a485a0011
running on linux-dit3 Sun Feb 23 20:56:33 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture:       x86_64
CPU op-mode(s):     32-bit, 64-bit
Byte Order:         Little Endian
CPU(s):             16
On-line CPU(s) list: 0–15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s):          2

(Continued on next page)
Cisco Systems
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Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
Stepping: 7
CPU MHz: 1900.000
CPU max MHz: 1900.0000
CPU min MHz: 1000.0000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15

Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpichs x87 smx mxv fxsr sse sse2 ss ht tm pbe syscall nx pdcgdb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdpl3 invpcid_single intel_pppin mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bni hle avx2 smep bmi2 3dnow mmx mtm cx16 movbe popcnt

tsc_deadline_timer_aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdpl_3 invpcid_single intel_pippin mba tpr_shadow vnmi flexpriority ept

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 385606 MB
node 0 free: 385026 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 387058 MB
node 1 free: 386610 MB
node distances:
node 0 1
0: 10 21
1: 21 10

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrate®2017_int_base = 55.0
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 791209240 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-dit3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted
Speculation, IBPB, IBRS_FW
run-level 3 Feb 23 20:48

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 btrfs 894G 9.4G 883G 2% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C240-M5L
Serial: WZP223909M5

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

Platform Notes (Continued)

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C                  | 502.gcc_r(peak) |
---|------------------|
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
| C                  | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak) |
---|-------------------|
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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| C                  | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak) |
---|-------------------|
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
| C++                | 523.xalancbmk_r(peak) |
---|---------------------|
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416

(Continued on next page)
## Compiler Version Notes (Continued)

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---

C++

| 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) |
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |

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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++

| 523.xalancbmk_r(peak) |

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

C++

| 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) |
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |

---

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

Fortran

| 548.exchange2_r(base, peak) |

---

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

## Base Compiler Invocation

C benchmarks:

```bash
icc -m64 -std=c11
```

C++ benchmarks:

```bash
icpc -m64
```

(Continued on next page)
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Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

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Copyright 2017-2020 Standard Performance Evaluation Corporation

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Test Date: Feb-2020
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Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=cl11

(Continued on next page)
Peak Compiler Invocation (Continued)


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

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<th>SPECrate®2017_int_base</th>
<th>55.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>56.1</td>
</tr>
</tbody>
</table>

Peak Optimization Flags (Continued)

505.mcf_r (continued):
- -lqkmalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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