## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)

<table>
<thead>
<tr>
<th>Threads</th>
<th>603.bwaves_s</th>
<th>607.cactuBSSN_s</th>
<th>619.lbm_s</th>
<th>621.wrf_s</th>
<th>627.cam4_s</th>
<th>628.pop2_s</th>
<th>638.imagick_s</th>
<th>644.nab_s</th>
<th>649.fotonik3d_s</th>
<th>654.roms_s</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
<td>56</td>
</tr>
<tr>
<td>SPECspeak®2017_fp_base = 153</td>
<td>SPECspeak®2017_fp_peak = 155</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test Date: | Feb-2020 |
| Hardware Availability: | Feb-2020 |
| Software Availability: | May-2019 |

### Hardware

- **CPU Name:** Intel Xeon Gold 6258R
- **Max MHz:** 4000
- **Nominal:** 2700
- **Enabled:** 56 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 38.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 960 GB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4j released Aug-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>56</td>
<td>115</td>
<td>513</td>
<td>56</td>
<td>115</td>
<td>512</td>
<td>56</td>
<td>115</td>
<td>512</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>56</td>
<td>88.6</td>
<td>188</td>
<td>89.0</td>
<td>187</td>
<td>56</td>
<td>88.7</td>
<td>188</td>
<td>89.2</td>
</tr>
<tr>
<td>619.ibm_s</td>
<td>56</td>
<td>49.8</td>
<td>105</td>
<td>51.9</td>
<td>101</td>
<td>50.0</td>
<td>105</td>
<td>51.0</td>
<td>104</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>56</td>
<td>102</td>
<td>130</td>
<td>102</td>
<td>130</td>
<td>102</td>
<td>130</td>
<td>98.4</td>
<td>134</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>56</td>
<td>71.6</td>
<td>124</td>
<td>71.9</td>
<td>123</td>
<td>71.6</td>
<td>124</td>
<td>71.2</td>
<td>123</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>56</td>
<td>213</td>
<td>55.7</td>
<td>215</td>
<td>55.3</td>
<td>212</td>
<td>56.1</td>
<td>212</td>
<td>56.5</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>56</td>
<td>86.1</td>
<td>168</td>
<td>82.6</td>
<td>175</td>
<td>83.2</td>
<td>173</td>
<td>80.3</td>
<td>180</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>56</td>
<td>52.6</td>
<td>332</td>
<td>52.6</td>
<td>332</td>
<td>52.6</td>
<td>332</td>
<td>52.6</td>
<td>332</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>56</td>
<td>106</td>
<td>86.3</td>
<td>105</td>
<td>86.7</td>
<td>105</td>
<td>86.5</td>
<td>105</td>
<td>86.3</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>56</td>
<td>97.9</td>
<td>161</td>
<td>99.2</td>
<td>159</td>
<td>99.1</td>
<td>159</td>
<td>99.7</td>
<td>161</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base** = 153  
**SPECspeed®2017_fp_peak** = 155

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)  

**SPEC CPU®2017 Floating Point Speed Result**

Copyright 2017-2020 Standard Performance Evaluation Corporation

---

**Table: Test Results**

<table>
<thead>
<tr>
<th>SPEC CPU®2017.fp.base</th>
<th>153</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPEC CPU®2017.fp.peak</td>
<td>155</td>
</tr>
</tbody>
</table>

---

**Platform Notes**

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1be6e46e485a0011
running on linux-dit3 Fri Feb 7 15:30:52 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 6258R CPU @ 2.70GHz
  2 "physical id"s (chips)
  56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
  physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
```

From lscpu:

```
Architecture:       x86_64
CPU op-mode(s):     32-bit, 64-bit
Byte Order:         Little Endian
CPU(s):             56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s):          2
NUMA node(s):       2
Vendor ID:          GenuineIntel
CPU family:         6
Model:              85
Model name:         Intel(R) Xeon(R) Gold 6258R CPU @ 2.70GHz
Stepping:           7
CPU MHz:            2700.000
CPU max MHz:        4000.0000
CPU min MHz:        1000.0000
BogoMIPS:           5400.00
Virtualization:     VT-x
```

(Continued on next page)
## Platform Notes (Continued)

- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 39424K
- **NUMA node0 CPU(s):** 0-27
- **NUMA node1 CPU(s):** 28-55
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_puin mba tpr_shadow vmmi flexpriority ept vpid fsgsb base tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdtd_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xsavec xgetbv1 xsavec cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

From `numactl --hardware` **WARNING:** a numactl 'node' might or might not correspond to a physical chip.

- **available:** 2 nodes (0-1)
  - **node 0 cpus:** 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
  - **node 0 size:** 385631 MB
  - **node 0 free:** 384760 MB
  - **node 1 cpus:** 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
  - **node 1 size:** 387025 MB
  - **node 1 free:** 379161 MB
  - **node distances:**
    - **node 0:** 10 21
    - **node 1:** 21 10

From `/proc/meminfo`

- **MemTotal:** 791201552 KB
- **HugePages_Total:** 0
- **Hugepagesize:** 2048 KB

From `/etc/*release* /etc/*version*`

- **os-release:**
  - **NAME**="SLES"
  - **VERSION**="15"
  - **VERSION_ID**="15"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)

SPECspeed®2017_fp_base = 153
SPECspeed®2017_fp_peak = 155

Platform Notes (Continued)

PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-dit3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 7 11:05

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
    Vendor: Cisco Systems Inc
    Product: UCSC-C240-M5L
    Serial: WZP223909M5

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>644.nab_s(base, peak)</th>
</tr>
</thead>
</table>

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
==============================================================================

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak) |
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak) |
==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11
(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)

SPECspeed®2017_fp_base = 153
SPECspeed®2017_fp_peak = 155

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves.s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
  -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)  

| SPECspeed®2017_fp_base = 153 |
| SPECspeed®2017_fp_peak = 155 |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Feb-2020  
Hardware Availability: Feb-2020  
Software Availability: May-2019

Base Optimization Flags (Continued)

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP  
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3  
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4  
-qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
## SPEC CPU®2017 Floating Point Speed Result

**Cisco Systems**
Cisco UCS C240 M5 (Intel Xeon Gold 6258R, 2.70GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>153</td>
<td>155</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Peak Optimization Flags (Continued)

654.roms_s (continued):
- `qopenmp`  
- `nostandard-realloc-lhs`

Benchmarks using both Fortran and C:

- 621.wrf_s: `-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512`  
  `-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div`  
  `-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp`  
  `-DSPEC_OPENMP -nostandard-realloc-lhs`

- 627.cam4_s: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`  
  `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`  
  `-DSPEC_OPENMP -nostandard-realloc-lhs`

- 628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`  
  `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`  
  `-DSPEC_OPENMP`  
  `-nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-02-07 15:30:51-0500.
Report generated on 2020-03-17 16:20:29 by CPU2017 PDF formatter v6255.
Originally published on 2020-03-17.