Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

<table>
<thead>
<tr>
<th>Copy</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>49.7</td>
<td>75.5</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>43.6</td>
<td>74.2</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>43.4</td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>47.9</td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>63.8</td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>73.8</td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>82.8</td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>54.6</td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>64.5</td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>66.8</td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>80.0</td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>95.9</td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>52.7</td>
<td></td>
</tr>
</tbody>
</table>

Hardware

- CPU Name: Intel Xeon Bronze 3206R
- Max MHz: 1900
- Nominal: 1900
- Enabled: 16 cores, 2 chips
- Orderable: 1,2 Chips
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 11 MB I+D on chip per chip
- Other: None
- Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)
- Storage: 1 x 960 GB SSD SAS
- Other: None

Software

- OS: SUSE Linux Enterprise Server 15 (x86_64)
- 4.12.14-23-default
- Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- Parallel: No
- Firmware: Version 4.0.4j released Aug-2019
- File System: btrfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: 64-bit
- Other: None
- Power Management: BIOS set to prefer performance at the cost of additional power usage

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Tested by: Cisco Systems
Test Sponsor: Cisco Systems
CPU2017 License: 9019
Hardware Availability: Feb-2020
Software Availability: May-2019

Page 1
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>16</td>
<td>555</td>
<td>289</td>
<td>555</td>
<td>289</td>
<td>554</td>
<td>290</td>
<td>556</td>
<td>289</td>
<td>554</td>
<td>290</td>
<td>556</td>
<td>289</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>16</td>
<td>407</td>
<td>49.7</td>
<td>423</td>
<td>47.8</td>
<td>407</td>
<td>49.7</td>
<td>419</td>
<td>49.7</td>
<td>420</td>
<td>49.7</td>
<td>420</td>
<td>49.7</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>16</td>
<td>354</td>
<td>43.0</td>
<td>354</td>
<td>43.0</td>
<td>354</td>
<td>43.0</td>
<td>354</td>
<td>43.0</td>
<td>354</td>
<td>43.0</td>
<td>354</td>
<td>43.0</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>16</td>
<td>873</td>
<td>47.9</td>
<td>874</td>
<td>47.9</td>
<td>875</td>
<td>47.9</td>
<td>874</td>
<td>47.9</td>
<td>875</td>
<td>47.9</td>
<td>874</td>
<td>47.9</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>16</td>
<td>584</td>
<td>63.9</td>
<td>587</td>
<td>63.6</td>
<td>586</td>
<td>63.8</td>
<td>586</td>
<td>63.8</td>
<td>587</td>
<td>63.6</td>
<td>586</td>
<td>63.8</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>16</td>
<td>246</td>
<td>68.4</td>
<td>246</td>
<td>68.5</td>
<td>246</td>
<td>68.5</td>
<td>246</td>
<td>68.5</td>
<td>246</td>
<td>68.5</td>
<td>246</td>
<td>68.5</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>16</td>
<td>432</td>
<td>83.0</td>
<td>434</td>
<td>82.7</td>
<td>433</td>
<td>82.8</td>
<td>433</td>
<td>82.8</td>
<td>432</td>
<td>83.0</td>
<td>432</td>
<td>83.0</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>16</td>
<td>445</td>
<td>54.7</td>
<td>446</td>
<td>54.6</td>
<td>446</td>
<td>54.6</td>
<td>446</td>
<td>54.6</td>
<td>446</td>
<td>54.6</td>
<td>446</td>
<td>54.6</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>16</td>
<td>434</td>
<td>64.5</td>
<td>434</td>
<td>64.5</td>
<td>434</td>
<td>64.5</td>
<td>434</td>
<td>64.5</td>
<td>434</td>
<td>64.5</td>
<td>434</td>
<td>64.5</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>16</td>
<td>294</td>
<td>135</td>
<td>292</td>
<td>136</td>
<td>292</td>
<td>136</td>
<td>292</td>
<td>136</td>
<td>292</td>
<td>136</td>
<td>292</td>
<td>136</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>16</td>
<td>336</td>
<td>80.1</td>
<td>337</td>
<td>79.9</td>
<td>336</td>
<td>80.0</td>
<td>336</td>
<td>80.0</td>
<td>336</td>
<td>80.1</td>
<td>336</td>
<td>80.1</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>16</td>
<td>650</td>
<td>95.9</td>
<td>650</td>
<td>95.9</td>
<td>651</td>
<td>95.8</td>
<td>651</td>
<td>95.8</td>
<td>650</td>
<td>95.9</td>
<td>650</td>
<td>95.9</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>16</td>
<td>485</td>
<td>52.4</td>
<td>480</td>
<td>52.9</td>
<td>482</td>
<td>52.7</td>
<td>484</td>
<td>52.5</td>
<td>481</td>
<td>52.8</td>
<td>478</td>
<td>53.2</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --bind=all runcpu
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

| SPECrate®2017_fp_base = 74.2 |
| SPECrate®2017_fp_peak = 75.5 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011
running on linux-dit3 Mon Feb 24 04:32:30 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>74.2</td>
<td>75.5</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Tested by:** Cisco Systems  
**Software Availability:** May-2019

## Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU family</td>
<td>6</td>
</tr>
<tr>
<td>Model</td>
<td>85</td>
</tr>
<tr>
<td>Model name</td>
<td>Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz</td>
</tr>
<tr>
<td>Stepping</td>
<td>7</td>
</tr>
<tr>
<td>CPU MHz:</td>
<td>1900.000</td>
</tr>
<tr>
<td>CPU max MHz:</td>
<td>1900.0000</td>
</tr>
<tr>
<td>CPU min MHz:</td>
<td>1000.0000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>3800.00</td>
</tr>
<tr>
<td>Virtualization:</td>
<td>VT-x</td>
</tr>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>11264K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-7</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>8-15</td>
</tr>
</tbody>
</table>
| Flags:                 | fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmm mba tpr_shadow vnumi flexpriority ept vptid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdts_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xsaveopt xsavec xsaveopt xstoreopt xsaveopt xreadopt xsavec xstoreopt xreadopt  
| /proc/cpuinfo cache data | cache size : 11264 KB |

From numactl --hardware  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.  
available: 2 nodes (0-1)  
node 0 cpus: 0 1 2 3 4 5 6 7  
node 0 size: 385606 MB  
node 0 free: 376755 MB  
node 1 cpus: 8 9 10 11 12 13 14 15  
node 1 size: 387058 MB  
node 1 free: 381886 MB  
node distances:  
node 0 1  
0: 10 21  
1: 21 10  

From /proc/meminfo  
MemTotal: 791209240 kB

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 74.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 75.5</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>Test Date:</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Feb-2020</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Hardware Availability:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Feb-2020</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tested by:</th>
<th>Software Availability:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

Platform Notes (Continued)

```
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From `/etc/*release*/etc/*version*`
```
os-release:
 NAME="SLES"
 VERSION="15"
 VERSION_ID="15"
 PRETTY_NAME="SUSE Linux Enterprise Server 15"
 ID="sles"
 ID_LIKE="suse"
 ANSI_COLOR="0;32"
 CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
 Linux linux-dit3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
 x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** No status reported
- **Microarchitectural Data Sampling:** No status reported
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

```
run-level 3 Feb 23 20:48
```

```
SPEC is set to: /home/cpu2017
 Filesystem     Type  Size  Used Avail Use% Mounted on
 /dev/sda1      btrfs  894G  21G  872G   3%   /home
```

```
From /sys/devices/virtual/dmi/id
 BIOS:     Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
 Vendor:   Cisco Systems Inc
 Product: UCSC-C240-M5L
 Serial:   WZP223909M5
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- **Memory:**
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

| SPECrate\textsuperscript{2017\_fp\_base} | = 74.2 |
| SPECrate\textsuperscript{2017\_fp\_peak} | = 75.5 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

C

| 519.lbm\_r(base, peak) 538.imagick\_r(base, peak) |
| 544.nab\_r(base, peak) |

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++

| 508.namd\_r(base, peak) 510.parest\_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C

| 511.povray\_r(base, peak) 526.blender\_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran

| 507.cactuBSSN\_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>74.2</td>
<td>75.5</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Compiler Version Notes (Continued)

<table>
<thead>
<tr>
<th>Fortran</th>
<th>503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
</tbody>
</table>
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>Fortran, C</th>
<th>521.wrf_r(base, peak) 527.cam4_r(base, peak)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td></td>
</tr>
</tbody>
</table>
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrates®2017 fp_base = 74.2
SPECrates®2017 fp_peak = 75.5

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrater®2017_fp_base = 74.2
SPECrater®2017_fp_peak = 75.5

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Sponsor</th>
<th>Tested by</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>9019</td>
<td>Cisco Systems</td>
<td>Cisco Systems</td>
<td>Feb-2020</td>
<td>Feb-2020</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 74.2**
**SPECrate®2017_fp_peak = 75.5**

---

### Peak Optimization Flags (Continued)

**510.parest_r**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

**503.bwaves_r**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

**549.fotonik3d_r**
Same as 503.bwaves_r

**554.roms_r**
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

**511.povray_r**
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

**526.blender_r**
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

---

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 74.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 75.5</td>
</tr>
</tbody>
</table>

### CPU2017 License: 9019

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Cisco Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Feb-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

---

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-02-24 04:32:28-0500.
Originally published on 2020-03-17.