Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 5.07
SPECspeed®2017_int_peak = 5.18

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler for Linux:
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4j released Aug-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage

Hardware
CPU Name: Intel Xeon Bronze 3206R
Max MHz: 1900
Nominal: 1900
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)
Storage: 1 x 960 GB SSD SAS
Other: None

Threads
<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base (5.07)</th>
<th>SPECspeed®2017_int_peak (5.18)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s 16</td>
<td>3.31</td>
</tr>
<tr>
<td>602.gcc_s 16</td>
<td>5.05</td>
</tr>
<tr>
<td>605.mcf_s 16</td>
<td>3.71</td>
</tr>
<tr>
<td>620.omnetpp_s 16</td>
<td>3.73</td>
</tr>
<tr>
<td>623.xalancbmk_s 16</td>
<td>6.17</td>
</tr>
<tr>
<td>625.x264_s 16</td>
<td>2.33</td>
</tr>
<tr>
<td>631.deepsjeng_s 16</td>
<td>2.87</td>
</tr>
<tr>
<td>641.leela_s 16</td>
<td>2.33</td>
</tr>
<tr>
<td>648.exchange2_s 16</td>
<td>8.1</td>
</tr>
<tr>
<td>657.xz_s 16</td>
<td>11.7</td>
</tr>
</tbody>
</table>

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019
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SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>16</td>
<td>535</td>
<td>3.32</td>
<td>537</td>
<td>3.31</td>
<td>537</td>
<td>3.31</td>
<td>16</td>
<td>456</td>
<td>3.89</td>
<td>458</td>
<td>3.88</td>
<td>456</td>
<td>3.89</td>
<td></td>
<td></td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>16</td>
<td>812</td>
<td>4.91</td>
<td>815</td>
<td>4.88</td>
<td>816</td>
<td>4.88</td>
<td>16</td>
<td>792</td>
<td>5.03</td>
<td>789</td>
<td>5.05</td>
<td>788</td>
<td>5.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>16</td>
<td>698</td>
<td>6.76</td>
<td>698</td>
<td>6.76</td>
<td>697</td>
<td>6.77</td>
<td>16</td>
<td>696</td>
<td>6.78</td>
<td>696</td>
<td>6.78</td>
<td>696</td>
<td>6.79</td>
<td></td>
<td></td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>16</td>
<td>438</td>
<td>3.72</td>
<td>440</td>
<td>3.71</td>
<td>439</td>
<td>3.71</td>
<td>16</td>
<td>436</td>
<td>3.74</td>
<td>441</td>
<td>3.70</td>
<td>438</td>
<td>3.73</td>
<td></td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>16</td>
<td>499</td>
<td>2.87</td>
<td>499</td>
<td>2.87</td>
<td>498</td>
<td>2.87</td>
<td>16</td>
<td>499</td>
<td>2.87</td>
<td>499</td>
<td>2.87</td>
<td>498</td>
<td>2.88</td>
<td></td>
<td></td>
</tr>
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<td>16</td>
<td>731</td>
<td>2.33</td>
<td>733</td>
<td>2.33</td>
<td>731</td>
<td>2.33</td>
<td>16</td>
<td>731</td>
<td>2.33</td>
<td>731</td>
<td>2.33</td>
<td>731</td>
<td>2.33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>16</td>
<td>528</td>
<td>11.7</td>
<td>527</td>
<td>11.7</td>
<td>527</td>
<td>11.7</td>
<td>16</td>
<td>520</td>
<td>11.9</td>
<td>520</td>
<td>11.9</td>
<td>520</td>
<td>11.9</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
SPEC CPU®2017 Integer Speed Result

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BIOS Settings:
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1b6e46a485a0011
running on linux-dit3 Mon Feb 24 20:32:47 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
 2 "physical id"s (chips)
 16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              16
On-line CPU(s) list: 0-15
Thread(s) per core:  1
Core(s) per socket:  8
Socket(s):           2
NUMA node(s):        2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
Stepping:            7
CPU MHz:             1900.000
CPU max MHz:         1900.0000
CPU min MHz:         1000.0000
BogoMIPS:            3800.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K

(Continued on next page)
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SPECspeed®2017_int_base = 5.07
SPECspeed®2017_int_peak = 5.18

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcd cca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdp_13 invpcid_single intel_puin mba tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdtp aavx512f aavx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xsavec xgetbv xsavecs cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospk aavx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size: 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 385635 MB
  node 0 free: 385153 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 387029 MB
  node 1 free: 386470 MB

From /proc/meminfo
  MemTotal: 791209240 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"

(Continued on next page)
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SPECspeed®2017_int_base = 5.07
SPECspeed®2017_int_peak = 5.18

Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-dit3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 24 20:30

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda1      btrfs 894G 16G  877G  2% /home

From /sys/devices/virtual/dmi/id
    BIOS:  Cisco Systems, Inc. C240M5.4.0.4j.0.0831191216 08/31/2019
    Vendor: Cisco Systems Inc
    Product: UCSC-C240-M5L
    Serial:  WZP223909M5

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
        24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
| C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak) |
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
## Cisco Systems
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| SPECspeed®2017_int_base = 5.07 |
| SPECspeed®2017_int_peak = 5.18 |

### Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------

- C++
  - 620.omnetpp_s(base, peak)
  - 623.xalancbmk_s(base, peak)
  - 631.deepsjeng_s(base, peak)
  - 641.leela_s(base, peak)

---------------------------------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------

- Fortran
  - 648.exchange2_s(base, peak)

---------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------

### Base Compiler Invocation

- **C benchmarks**:  
  - icc -m64 -std=c11

- **C++ benchmarks**:  
  - icpc -m64

- **Fortran benchmarks**:  
  - ifort -m64

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64

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## Cisco Systems
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**SPECspeed®2017_int_base = 5.07**  
**SPECspeed®2017_int_peak = 5.18**

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<tr>
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<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Base Portability Flags (Continued)

657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
- L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**
- Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

**Fortran benchmarks:**
- xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
- nostandard-realloc-lhs

### Peak Compiler Invocation

**C benchmarks:**
icc -m64 -std=c11

**C++ benchmarks:**
icpc -m64

**Fortran benchmarks:**
ifort -m64

### Peak Portability Flags

Same as Base Portability Flags
## Cisco Systems
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### SPEC CPU®2017 Integer Speed Result

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**SPECspeed®2017_int_base = 5.07**
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### CPU2017 License: 9019

### Peak Optimization Flags

C benchmarks:

600.perlbench_s:
- `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`
- `-no-prec-div -DSPC_SUPPRESS_OPENMP -gopenmp`
- `-DSPC_OPENMP -fno-strict-overflow`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

602.gcc_s:
- `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`
- `-no-prec-div -DSPC_SUPPRESS_OPENMP`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

605.mcf_s:
- `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo`
- `-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4`
- `-DSPC_SUPPRESS_OPENMP -gopenmp -DSPC_OPENMP`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

625.x264_s:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -gopenmp -DSPC_OPENMP`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

657.xz_s:
- `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`
- `-no-prec-div -DSPC_SUPPRESS_OPENMP -gopenmp`
- `-DSPC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc`

C++ benchmarks:

620.omnetpp_s:
- `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo`
- `-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4`
- `-DSPC_SUPPRESS_OPENMP`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

623.xalancbk_s:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

631.deepsjeng_s: Same as 623.xalancbk_s

641.leela_s: Same as 623.xalancbk_s

Fortran benchmarks:

- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`

*(Continued on next page)*
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Peak Optimization Flags (Continued)

Fortran benchmarks (continued):
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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