Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

SPECrater®2017_int_base = 284
SPECrater®2017_int_peak = 297

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

<table>
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<tr>
<th>SPECrate®2017_int_base (284)</th>
<th>SPECrate®2017_int_peak (297)</th>
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</thead>
</table>

**SPECrater®2017_int_base = 284**

**SPECrater®2017_int_peak = 297**

| Copies | 0 | 30.0 | 60.0 | 90.0 | 120 | 150 | 180 | 210 | 240 | 270 | 300 | 330 | 360 | 390 | 420 | 450 | 480 | 510 | 540 | 570 | 600 | 630 |
|--------|---|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 500.perlbench_r | 104 | 221 | 255 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 502.gcc_r | 104 | 227 | 266 | 357 | 357 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 505.mcf_r | 104 |      | 182 | 183 | 295 | 324 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 520.omnetpp_r | 104 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 523.xalancbmk_r | 104 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 525.x264_r | 104 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 531.deepsjeng_r | 104 | 233 | 232 | 230 | 592 | 591 |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 541.leela_r | 104 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 548.exchange2_r | 104 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 557.xz_r | 104 |      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Software**

**OS:** SUSE Linux Enterprise Server 15 (x86_64)

**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;

Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux

**Firmware:** version 4.0.4i released Aug-2019

**File System:** btrfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** 32/64-bit

**Other:** jemalloc memory allocator V5.0.1

**Power Management:** BIOS set to prefer performance at the cost of additional power usage

---

**Hardware**

**CPU Name:** Intel Xeon Gold 6230R

**Max MHz:** 4000

**Nominal:** 2100

**Enabled:** 52 cores, 2 chips, 2 threads/core

**Orderable:** 1.2 Chips

**Cache L1:** 32 KB I + 32 KB D on chip per core

**L2:** 1 MB I+D on chip per core

**L3:** 35.75 MB I+D on chip per chip

**Other:** None

**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)

**Storage:** 1 x 960 GB SSD SAS

**Other:** None
## Results Table

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<th>Seconds</th>
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<th>Seconds</th>
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</tr>
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**SPECrate®2017_int_base = 284**

**SPECrate®2017_int_peak = 297**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```bash
sync; echo 3>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011
running on linux-4lf8 Sun Feb 16 23:41:21 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6230R CPU @ 2.10GHz
  2 "physical id"s (chips)
  104 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 26
  siblings : 52
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 104
On-line CPU(s) list: 0-103

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

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CPU2017 License: 9019
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Test Date: Feb-2020
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Software Availability: May-2019

---

**Platform Notes (Continued)**

Thread(s) per core: 2
Core(s) per socket: 26
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6230R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2100.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,20-22,52-55,59-61,65-67,72-74
NUMA node1 CPU(s): 4-6,10-12,16-19,23-25,56-58,62-64,68-71,75-77
NUMA node2 CPU(s): 26-29,33-35,39-41,46-48,78-81,85-87,91-93,98-100
NUMA node3 CPU(s): 30-32,36-38,42-45,49-51,82-84,88-90,94-97,101-103
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep goodnop lmxtechnology nonstop_tsc cpuid
aperfmrperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdgdb fma cx16 xtpr pdcml dca ssse4_1 ssse4_2 x2apic movbe popcnt
/proc/cpuinfo cache data
   cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 13 14 15 20 21 22 52 53 54 55 59 60 61 65 66 67 72 73 74
node 0 size: 192101 MB
node 0 free: 191562 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 19 23 24 25 56 57 58 62 63 64 68 69 70 71 75 76 77
node 1 size: 193525 MB
node 1 free: 193093 MB

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

node 2 cpus: 26 27 28 29 33 34 35 39 40 41 46 47 48 78 79 80 81 85 86 87 91 92 93 98 99 100
node 2 size: 193525 MB
node 2 free: 193290 MB
node 3 cpus: 30 31 32 36 37 38 42 43 44 45 49 50 51 82 83 84 88 89 90 94 95 96 97 101 102 103
node 3 size: 193494 MB
node 3 free: 193261 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791191332 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*

```
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
run-level 3 Feb 16 23:04
```
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Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 284
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CPU2017 License: 9019
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Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdd1 btrfs 559G 9.2G 548G 2% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C220M5.4.0.4i.0.0831191119 08/31/2019
Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP22380Z2S

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

------------------------------------------
C | 502.gcc_r(peak)
------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------

------------------------------------------
C | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
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**Compiler Version Notes (Continued)**

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| C++      | omnetpp_r(base, peak) |  |
|          | xalancbmk_r(base) |  |
|          | deepsjeng_r(base, peak) |  |
|          | leela_r(base, peak) |  |
| Intel(R) C++ | Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

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| Intel(R) C++ | Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |

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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-transform=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-transform=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

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Software Availability: May-2019

**Base Optimization Flags (Continued)**

C++ benchmarks (continued):
- -lqkmalloc

Fortran benchmarks:
- -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte  
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

**Peak Compiler Invocation**

C benchmarks (except as noted below):
- icc -m64 -std=c11  

C++ benchmarks (except as noted below):
- icpc -m64  
- 523xalancbmk_r: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
- ifort -m64

**Peak Portability Flags**

- 500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
- 502.gcc_r: -D_FILE_OFFSET_BITS=64  
- 505.mcf_r: -DSPEC_LP64  
- 520.omnetpp_r: -DSPEC_LP64  
- 523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
- 525.x264_r: -DSPEC_LP64  
- 531.deepsjeng_r: -DSPEC_LP64  
- 541.leela_r: -DSPEC_LP64  
- 548.exchange2_r: -DSPEC_LP64  
- 557.xz_r: -DSPEC_LP64
## SPEC CPU®2017 Integer Rate Result

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### Peak Optimization Flags

#### C benchmarks:

500.perlbench_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

502.gcc_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc


557.xz_r: Same as 505.mcf_r

#### C++ benchmarks:


523.xalancbmk_r: `-Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

#### Fortran benchmarks:

# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

### Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

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<tr>
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The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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