## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Feb-2020</td>
<td>Feb-2020</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Tested by:** Cisco Systems  
**Hardware:**
- **CPU Name:** Intel Xeon Gold 6230R  
- **Max MHz:** 4000  
- **Nominal:** 2100  
- **Enabled:** 52 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **Cache L2:** 1 MB I+D on chip per core  
- **Cache L3:** 35.75 MB I+D on chip per chip  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 960 GB SSD SAS  
- **Other:** None  

**Software:**
- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4i released Aug-2019  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  

**Power Management:** BIOS set to prefer performance at the cost of additional power usage

### SPEC CPU 2017 Floating Point Rate Result

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<th>Copy</th>
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<th>SPECrate®2017_fp_peak</th>
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## Results Table

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</tr>
</tbody>
</table>

SPECrate®2017_fp_base = 247

SPECrate®2017_fp_peak = 251

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

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Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

SPECrate®2017_fp_base = 247
SPECrate®2017_fp_peak = 251

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
running on linux-41f8 Mon Feb 17 09:00:49 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6230R CPU @ 2.10GHz
2 "physical id"s (chips)
104 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 26
siblings : 52
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 22 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 104
On-line CPU(s) list: 0-103
Thread(s) per core: 2
Core(s) per socket: 26

(Continued on next page)
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SPECrate®2017_fp_base = 247
SPECrate®2017_fp_peak = 251

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6230R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2100.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,20-22,52-55,59-61,65-67,72-74
NUMA node1 CPU(s): 4-6,10-12,16-19,23-25,56-58,62-64,68-71,75-77
NUMA node2 CPU(s): 26-29,33-35,39-41,46-48,78-81,85-87,91-93,98-100
NUMA node3 CPU(s): 30-32,36-38,42-45,49-51,82-84,88-90,94-97,101-103
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr perfctr0 perfctr1 perfctr2 perfctr3 perfctr4 perfctr5 perfctr6 perfctr7 perfctr8 perfctr9 perfctr10 perfctr11 perfctr12 perfctr13 perfctr14 perfctr15 perfctr16 perfctr17 perfctr18 perfctr19 perfctr20 perfctr21 perfctr22 perfctr23 perfctr24 perfctr25 perfctr26 perfctr27 perfctr28 perfctr29 perfctr30 perfctr31 perfctr32 perfctr33 perfctr34 perfctr35 perfctr36 perfctr37 perfctr38 perfctr39 perfctr40 perfctr41 perfctr42 perfctr43 perfctr44 perfctr45 perfctr46 perfctr47 perfctr48 perfctr49 perfctr50 perfctr51 perfctr52 perfctr53 perfctr54 perfctr55 perfctr56 perfctr57 perfctr58 perfctr59 perfctr60 perfctr61 perfctr62 perfctr63 perfctr64 perfctr65 perfctr66 perfctr67 perfctr68 perfctr69 perfctr70 perfctr71 perfctr72 perfctr73 perfctr74 perfctr75 perfctr76 perfctr77 perfctr78 perfctr79 perfctr80 perfctr81 perfctr82 perfctr83 perfctr84 perfctr85 perfctr86 perfctr87 perfctr88 perfctr89 perfctr90 perfctr91 perfctr92 perfctr93 perfctr94 perfctr95 perfctr96 perfctr97 perfctr98 perfctr99 perfctr100 perfctr101 perfctr102 perfctr103 perfctr104 perfctr105 perfctr106 perfctr107 perfctr108 perfctr109 perfctr110 perfctr111 perfctr112 perfctr113 perfctr114 perfctr115 perfctr116 perfctr117 perfctr118 perfctr119 perfctr120 perfctr121 perfctr122 perfctr123 perfctr124 perfctr125 perfctr126 perfctr127 perfctr128 perfctr129 perfctr130 perfctr131 perfctr132 perfctr133 perfctr134 perfctr135 perfctr136 perfctr137 perfctr138 perfctr139 perfctr140 perfctr141 perfctr142 perfctr143 perfctr144 perfctr145 perfctr146 perfctr147 perfctr148 perfctr149 perfctr150 perfctr151 perfctr152 perfctr153 perfctr154 perfctr155 perfctr156 perfctr157 perfctr158 perfctr159 perfctr160 perfctr161 perfctr162 perfctr163 perfctr164 perfctr165 perfctr166 perfctr167 perfctr168 perfctr169 perfctr170 perfctr171 perfctr172 perfctr173 perfctr174 perfctr175 perfctr176 perfctr177 perfctr178 perfctr179 perfctr180 perfctr181 perfctr182 perfctr183 perfctr184 perfctr185 perfctr186 perfctr187 perfctr188 perfctr189 perfctr190 perfctr191 perfctr192 perfctr193 perfctr194 perfctr195 perfctr196 perfctr197 perfctr198 perfctr199 perfctr200 perfctr201 perfctr202 perfctr203 perfctr204 perfctr205 perfctr206 perfctr207 perfctr208 perfctr209 perfctr210 perfctr211 perfctr212 perfctr213 perfctr214 perfctr215 perfctr216 perfctr217 perfctr218 perfctr219 perfctr220 perfctr221 perfctr222 perfctr223 perfctr224 perfctr225 perfctr226 perfctr227 perfctr228 perfctr229 perfctr230 perfctr231 perfctr232 perfctr233 perfctr234 perfctr235 perfctr236 perfctr237 perfctr238 perfctr239 perfctr240 perfctr241 perfctr242 perfctr243 perfctr244 perfctr245 perfctr246 perfctr247 perfctr248 perfctr249 perfctr250 perfctr251 perfctr252 perfctr253 perfctr254 perfctr255

/proc/cpuinfo cache data
  cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 7 8 9 13 14 15 20 21 22 52 53 54 55 59 60 61 65 66 67 72 73 74
  node 0 size: 192101 MB
  node 0 free: 177937 MB
  node 1 cpus: 4 5 6 10 11 12 16 17 18 19 23 24 25 56 57 58 62 63 64 68 69 70 71 75 76 77
  node 1 size: 193525 MB
  node 1 free: 182689 MB
  node 2 cpus: 26 27 28 29 33 34 35 39 40 41 46 47 48 78 79 80 81 85 86 87 91 92 93 98 99
  100

(Continued on next page)
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Platform Notes (Continued)

node 2 size: 193525 MB
node 2 free: 182664 MB
node 3 cpus: 30 31 32 36 37 38 42 43 44 45 49 50 51 82 83 84 88 89 90 94 95 96 97 101 102 103
node 3 size: 193494 MB
node 3 free: 182962 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791191332 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-4lf8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 16 23:04

SPEC is set to: /home/cpu2017

(Continued on next page)
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Platform Notes (Continued)

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<th>Type</th>
<th>Size</th>
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<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
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<tbody>
<tr>
<td>/dev/sdd1</td>
<td>btrfs</td>
<td>559G</td>
<td>52G</td>
<td>508G</td>
<td>10%</td>
<td>/home</td>
</tr>
</tbody>
</table>

From /sys/devices/virtual/dmi/id
BIOS:  Cisco Systems, Inc. C220M5.4.0.4i.0.0831191119 08/31/2019
Vendor:  Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial:  WZP22380ZZS

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C
| 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
| 508.namd_r(base, peak) 510.parest_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C
| 511.povray_r(base, peak) 526.blender_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

| SPECrate®2017_fp_base = 247 |
| SPECrate®2017_fp_peak = 251 |

| CPU2017 License: | 9019 |
| Test Sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test Date: | Feb-2020 |
| Hardware Availability: | Feb-2020 |
| Software Availability: | May-2019 |

**Compiler Version Notes (Continued)**

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C++, C, Fortran | 507.cactuBSSN_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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**Base Compiler Invocation**

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```
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SPEC CPU®2017 Floating Point Rate Result
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Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
527.cam4_r: -DSPEC_LP64
528.imagick_r: -DSPEC_LP64 -DSPEC_LP64
544.nab_r: -DSPEC_LP64 -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

SPECrater®2017_fp_base = 247
SPECrater®2017_fp_peak = 251

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)  SPECrate®2017_fp_base = 247
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CPU2017 License: 9019
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Software Availability: May-2019

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
544.nab_r: Same as 538.imagick_r

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte
549.fotonik3d_r: Same as 503.bwaves_r
554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

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Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6230R, 2.10GHz)  

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Peak Optimization Flags (Continued)

526.blender_f: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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