**SPEC CPU®2017 Floating Point Speed Result**

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(3.40 GHz, Intel Xeon Gold 6246R)

### SPECspeed®2017_fp_base = 146

### SPECspeed®2017_fp_peak = 146

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Mar-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability:</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Jun-2019</td>
</tr>
</tbody>
</table>

#### Hardware

- **CPU Name:** Intel Xeon Gold 6246R  
- **Max MHz:** 4100  
- **Nominal:** 3400  
- **Enabled:** 32 cores, 2 chips  
- **Orderable:** 1, 2 chip(s)  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 35.75 MB I+D on chip per chip  
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2933Y-R)  
- **Storage:** 1 x 400 GB SAS SSD, RAID 0  
- **Other:** None  

<table>
<thead>
<tr>
<th>Software</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OS:</strong></td>
<td>SUSE Linux Enterprise Server 15 SP1 (x86_64)</td>
</tr>
<tr>
<td><strong>Kernel:</strong></td>
<td>4.12.14-195-default</td>
</tr>
<tr>
<td><strong>Compiler:</strong></td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;</td>
</tr>
<tr>
<td><strong>Parallel:</strong></td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Firmware:</strong></td>
<td>HPE BIOS Version I42 v2.22 (11/13/2019) released Feb-2020</td>
</tr>
<tr>
<td><strong>File System:</strong></td>
<td>btrfs</td>
</tr>
<tr>
<td><strong>System State:</strong></td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td><strong>Base Pointers:</strong></td>
<td>64-bit</td>
</tr>
<tr>
<td><strong>Peak Pointers:</strong></td>
<td>64-bit</td>
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<tr>
<td><strong>Other:</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>Power Management:</strong></td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>

#### Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>146 threads</th>
<th>32 threads</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>151</td>
<td>549</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>151</td>
<td>34</td>
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<tr>
<td>619.lbm_s</td>
<td>104</td>
<td>70</td>
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<tr>
<td>621.wrf_s</td>
<td>146</td>
<td>123</td>
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<tr>
<td>627.cam4_s</td>
<td>95.2</td>
<td>25</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>72.9</td>
<td>72.9</td>
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<tr>
<td>638.imagick_s</td>
<td>127</td>
<td>126</td>
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<tr>
<td>644.nab_s</td>
<td>243</td>
<td>243</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>86.3</td>
<td>86.4</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>183</td>
<td>183</td>
</tr>
</tbody>
</table>

---

Copyright 2017-2020 Standard Performance Evaluation Corporation
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
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<td>552</td>
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<td>607.cactubssn_s</td>
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<td>619.lbm_s</td>
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<td>90.8</td>
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<td>85.6</td>
<td>184</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Operating System Notes

- Stack size set to unlimited using "ulimit -s unlimited"
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```
  sync; echo 3>/proc/sys/vm/drop_caches
  ```

### Environment Variables Notes

- Environment variables set by runcpu before the start of the run:
  ```
  KMP_AFFINITY = "granularity=fine,compact"
  LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
  OMP_STACKSIZE = "192M"
  ```

### General Notes

- Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
- NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(3.40 GHz, Intel Xeon Gold 6246R)

SPECspeak®2017_fp_base = 146
SPECspeak®2017_fp_peak = 146

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Energy/Performance Bias set to Balanced Power
Workload Profile set to Custom
Numa Group Size Optimization set to Flat
Intel UPI Link Power Management set to Enabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed6e6e46a485a0011
running on sy480-sys2 Sun Mar 1 00:35:09 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 1 2 3 9 12 13 16 17 18 19 22 26 27 28 29
physical 1: cores 0 1 2 3 5 6 9 11 12 16 18 19 20 26 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz

(Continued on next page)
**Hewlett Packard Enterprise**  
*Test Sponsor: HPE*  
**Synergy 480 Gen10**  
*(3.40 GHz, Intel Xeon Gold 6246R)*

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<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>146</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

- **Stepping:** 7
- **CPU MHz:** 3400.000
- **BogoMIPS:** 6800.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 36608K
- **NUMA node0 CPU(s):** 0-15
- **NUMA node1 CPU(s):** 16-31
- **Flags:** fpu vme de pse tsc msr pae mce cmov cmov apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpes1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pme ssbd mba ibrs ibpb ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavecv xsavec xsavecs cqm_llc cqm_occum_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data

```
cache size : 36608 KB
```

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
 available: 2 nodes (0-1)  
n 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
n 0 size: 193025 MB  
n 0 free: 192453 MB  
n 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31  
n 1 size: 193336 MB  
n 1 free: 193125 MB  
n 0 distances:  
n 0 1  
 0: 10 21  
 1: 21 10
```

From /proc/meminfo

```
MemTotal:          395634796 kB
HugePages_Total:       0
Hugepagesize:          2048 KB
```

From /etc/*release* /etc/*version*

```
os-release:
```

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Hewlett Packard Enterprise  
**Synergy 480 Gen10**  
(3.40 GHz, Intel Xeon Gold 6246R)  

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Test Date</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

**SPEC CPU®2017 Floating Point Speed Result**

**SPECspeed®2017_fp_base = 146**

**SPECspeed®2017_fp_peak = 146**

Platform Notes (Continued)

```bash
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"
```

```bash
uname -a:
Linux sy480-sys2 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516) x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

```
run-level 3 Mar 1 00:33
```

```
SPEC is set to: /home/cpu2017
```

```
Filesystem  Type     Size  Used  Avail Use% Mounted on
/dev/sda2  btrfs     371G   24G  346G   7% /home
```

From `/sys/devices/virtual/dmi/id`

- **BIOS:** HPE I42 11/13/2019
- **Vendor:** HPE
- **Product:** Synergy 480 Gen10
- **Product Family:** Synergy
- **Serial:** MXQ7380505

Additional information from `dmidecode` follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
Memory:
  24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933
```

(End of data from `sysinfo` program)
Hewlett Packard Enterprise
Synergy 480 Gen10
(3.40 GHz, Intel Xeon Gold 6246R)

CPU2017 License: 3
Test Sponsor: HPE
Test Date: Mar-2020
Tested by: HPE
Hardware Availability: Feb-2020
Software Availability: Jun-2019

SPECspeed®2017_fp_base = 146
SPECspeed®2017_fp_peak = 146

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

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Test Date: Mar-2020
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Base Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs
649.fotonik3d_s: Same as 603.bwaves_s
654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Hewlett Packard Enterprise
Synergy 480 Gen10
(3.40 GHz, Intel Xeon Gold 6246R)

SPECspeed\textsuperscript{®}2017\_fp\_base = 146
SPECspeed\textsuperscript{®}2017\_fp\_peak = 146

Peak Optimization Flags (Continued)

654.\textit{roms\_s} (continued):
\texttt{-qopenmp -nostandard-realloc-lhs}

Benchmarks using both Fortran and C:

621.\textit{wrf\_s}: \texttt{-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -DSPEC\textunderscore SUPPRESS\textunderscore OPENMP -qopenmp -DSPEC\textunderscore OPENMP -nostandard-realloc-lhs}

627.\textit{cam4\_s}: \texttt{-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC\textunderscore OPENMP -nostandard-realloc-lhs}

628.\textit{pop2\_s}: Same as 621.\textit{wrf\_s}

Benchmarks using Fortran, C, and C++:

\texttt{-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC\textunderscore OPENMP -nostandard-realloc-lhs}

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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