### SPEC CPU®2017 Integer Speed Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10  
(2.40 GHz, Intel Xeon Silver 4214R)

| SPECspeed®2017_int_base = 8.58 | SPECspeed®2017_int_peak = 8.70 |

**CPU2017 License:** 3  
**Test Date:** Mar-2020  
**Test Sponsor:** HPE  
**Hardware Availability:** Feb-2020  
**Tested by:** HPE  
**Software Availability:** Jun-2019

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
</table>
| **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
Kernel 4.12.14-195-default  
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++  
Compiler Build 20190416 for Linux;  
Fortran: Version 19.0.4.227 of Intel Fortran  
Compiler Build 20190416 for Linux;  
Parallel: Yes  
Firmware: HPE BIOS Version U30 v2.22 (11/13/2019) released Feb-2020  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 64-bit  
Other: jemalloc memory allocator V5.0.1  
Power Management: BIOS set to prefer performance at the cost of additional power usage |

| **CPU Name:** Intel Xeon Silver 4214R  
**Max MHz:** 3500  
**Nominal:** 2400  
**Enabled:** 24 cores, 2 chips  
**Orderable:** 1, 2 chip(s)  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 16.5 MB I+D on chip per chip  
**Other:** None  
**Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)  
**Storage:** 1 x 400 GB SAS SSD  
**Other:** None |

| Threads | 0 | 1.00 | 2.00 | 3.00 | 4.00 | 5.00 | 6.00 | 7.00 | 8.00 | 9.00 | 10.0 | 11.0 | 12.0 | 13.0 | 14.0 | 15.0 | 16.0 | 17.0 | 18.0 | 19.0 |
|---------|---|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 600.perlbench_s | 24 | 6.61 | | | | | | | | | | | | | | | | | | |
| 602.gcc_s | 24 | 8.34 | | | | | | | | | | | | | | | | | | |
| 605.mcf_s | 24 | 8.44 | | | | | | | | | | | | | | | | | | |
| 620.omnetpp_s | 24 | 6.06 | | | | | | | | | | | | | | | | | | |
| 623.xalancbmk_s | 24 | 5.39 | | | | | | | | | | | | | | | | | | |
| 625.x264_s | 24 | | | | | | | | | | | | | | | | | | |
| 631.deepsjeng_s | 24 | 4.88 | | | | | | | | | | | | | | | | | | |
| 641.leela_s | 24 | 4.10 | | | | | | | | | | | | | | | | | | |
| 648.exchange2_s | 24 | | | | | | | | | | | | | | | | | | |
| 657.xz_s | 24 | | | | | | | | | | | | | | | | | | |

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**Figure:** SPECspeed®2017 Int Result

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**Note:**
- CPU2017 License: 3
- Test Sponsor: HPE
- Hardware Availability: Feb-2020
- Tested by: HPE
- Software Availability: Jun-2019

---

**Results:**
- SPECspeed®2017_int_base = 8.58
- SPECspeed®2017_int_peak = 8.70

---

**Threads:**
- 600.perlbench_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 602.gcc_s: 24 threads, SPECspeed®2017_int_peak = 8.70
- 605.mcf_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 620.omnetpp_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 623.xalancbmk_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 625.x264_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 631.deepsjeng_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 641.leela_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 648.exchange2_s: 24 threads, SPECspeed®2017_int_base = 8.58
- 657.xz_s: 24 threads, SPECspeed®2017_int_base = 8.58

---

**Additional Information:**
- CPU Name: Intel Xeon Silver 4214R
- Max MHz: 3500
- Nominal: 2400
- Enabled: 24 cores, 2 chips
- Orderable: 1, 2 chip(s)
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 16.5 MB I+D on chip per chip
- Other: None
- Memory: 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)
- Storage: 1 x 400 GB SAS SSD
- Other: None
Results Table

<table>
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<th>Benchmark</th>
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<td><strong>329</strong></td>
<td><strong>18.8</strong></td>
<td>329</td>
<td>18.8</td>
</tr>
</tbody>
</table>

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3 > /proc/sys/vm/drop_caches

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
    KMP_AFFINITY = "granularity=granularity=fine,compact"
    LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
    OMP_STACKSIZE = "192M"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
General Notes (Continued)

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Power
Minimum Processor Idle Power Core C-State set to C1E State
Numa Group Size Optimization set to Flat
XPT Prefetcher set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbb6e46a485a0011
running on linux-r6ge Sat Mar 7 12:53:39 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
  2 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
  physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
  physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 24
On-line CPU(s) list: 0-23

(Continued on next page)
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SPECspeed®2017_int_base = 8.58
SPECspeed®2017_int_peak = 8.70

Platform Notes (Continued)

Thread(s) per core:  1
Core(s) per socket:  12
Socket(s):  2
NUMA node(s):  2
Vendor ID:  GenuineIntel
CPU family:  6
Model:  85
Model name:  Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
Stepping:  7
CPU MHz:  2400.000
BogoMIPS:  4800.00
Virtualization:  VT-x
L1d cache:  32K
L1i cache:  32K
L2 cache:  1024K
L3 cache:  16896K
NUMA node0 CPU(s):  0-11
NUMA node1 CPU(s):  12-23
Flags:  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_patin ssbd mbb ibpb stibp ibrs Enhanced tpr_shadow vmvi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total
cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
arch_capabilities

/proc/cpuinfo cache data
cache size : 16896 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
node 0 size: 193128 MB
node 0 free: 190763 MB
node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
node 1 size: 193503 MB
node 1 free: 193248 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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ProLiant DL380 Gen10
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SPECspeed®2017_int_base = 8.58
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 395911256 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-r6ge 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 7 12:51

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 371G 148G 223G 40% /home

From /sys/devices/virtual/dmi/id
BIOS: HPE U30 11/13/2019
Vendor: HPE
Product: ProLiant DL380 Gen10
Product Family: ProLiant
Serial: 2M294204YX

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow
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(Test Sponsor: HPE)
ProLiant DL380 Gen10
(2.40 GHz, Intel Xeon Silver 4214R)

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Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

 Platform Notes (Continued)

hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

 Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)</th>
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<tbody>
<tr>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
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<tr>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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<td>------------------------------------------------------------------------------------------------------------------</td>
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<td>C++</td>
<td>620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)</td>
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<td>Fortran</td>
<td>648.exchange2_s(base, peak)</td>
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 Base Compiler Invocation

C benchmarks:
```bash
icc -m64 -std=c11
```

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```
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**Test Date:** Mar-2020  
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### Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
602.gcc_s: -DSPEC_LP64  
605.mcf_s: -DSPEC_LP64  
620.omnetpp_s: -DSPEC_LP64  
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leela_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
- -L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=4  
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
- -lqkmalloc

**Fortran benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
- -nostandard-realloc-lhs

### Peak Compiler Invocation

**C benchmarks:**
- icc -m64 -std=c11

**C++ benchmarks:**
- icpc -m64

**Fortran benchmarks:**
- ifort -m64
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Copyright 2017-2020 Standard Performance Evaluation Corporation

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CPU2017 License: 3
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Test Date: Mar-2020
Hardware Availability: Feb-2020
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Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10
(2.40 GHz, Intel Xeon Silver 4214R)

SPECspeed®2017_int_base = 8.58
SPECspeed®2017_int_peak = 8.70

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 623.xalancbmk_s
641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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