## SPEC CPU®2017 Integer Rate Result

**Copyright 2017-2020 Standard Performance Evaluation Corporation**

### Hewlett Packard Enterprise

**Test Sponsor:** HPE  
**ProLiant DL380 Gen10**  
**CPU Type:** 3.20 GHz, Intel Xeon Silver 4215R

### SPECrate®2017_int_base = 105

### SPECrate®2017_int_peak = 110

#### CPU2017 License:
- 3

#### Test Date:
- Mar-2020

#### Test Sponsor:
- HPE

#### Hardware Availability:
- Feb-2020

#### Tested by:
- HPE

#### Software Availability:
- Jun-2019

#### Tested Date:
- Mar-2020

#### Hardware Availability:
- Feb-2020

#### Tested by:
- HPE

#### Software Availability:
- Jun-2019

#### Hardware

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#### Software

**CPU Name:** Intel Xeon Silver 4215R  
**Max MHz:** 4000  
**Nominal:** 3200  
**Enabled:** 16 cores, 2 chips, 2 threads/core  
**Orderable:** 1, 2 chip(s)  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 11 MB I+D on chip per core  
**Orderable:** None  
**Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)  
**Storage:** 1 x 400 GB SAS SSD  
**Other:** None  

**OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
**Kernel:** 4.12.14-195-default  
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;  

**Parallel:** No  
**Firmware:** HPE BIOS Version U30 v2.16 (09/12/2019) released Feb-2020  
**File System:** btrfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 32/64-bit  
**Other:** jemalloc memory allocator V5.0.1  
**Power Management:** BIOS set to prefer performance at the cost of additional power usage
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

SPEC CPU®2017 Integer Rate Result
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SPECrate®2017_int_base = 105
SPECrate®2017_int_peak = 110

Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3 >       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
  "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

<table>
<thead>
<tr>
<th>CPU2017 License: 3</th>
<th>Test Date: Mar-2020</th>
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<tr>
<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Feb-2020</td>
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<td>Tested by: HPE</td>
<td>Software Availability: Jun-2019</td>
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</table>

**SPEC CPU®2017 Integer Rate Result**
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**SPECrate®2017_int_peak = 110**
**SPECrate®2017_int_base = 105**

General Notes (Continued)

memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Power

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb661e46a485a0011
running on linux-3rlx Mon Mar 9 14:20:27 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64

(Continued on next page)
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ProLiant DL380 Gen10
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SPECrate®2017_int_base = 105
SPECrate®2017_int_peak = 110

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
Stepping: 7
CPU MHz: 3200.000
BogoMIPS: 6400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7,16-23
NUMA node1 CPU(s): 8-15,24-31

Flags:
  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
  lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
  xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
  avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
  invpcid_single intel_pmm ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
  flexpriority etp vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtmt
  cmx mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
  avx512bw avx512vli xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
  cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
  arch_capabilities

/proc/cpuinfo cache data
  cache size: 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
  node 0 size: 193090 MB
  node 0 free: 190726 MB
  node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
  node 1 size: 193532 MB

(Continued on next page)
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes (Continued)

node 1 free: 193116 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 395901804 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-3rlx 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 9 14:17

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 369G 182G 186G 50% /home

From /sys/devices/virtual/dmi/id
BIOS: HPE U30 09/12/2019
Vendor: HPE
Product: ProLiant DL380 Gen10

(Continued on next page)
<table>
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<td>Serial: 2M294204YV</td>
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Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 12x UNKNOWN NOT AVAILABLE
- 12x UNKNOWN NOT AVAILABLE 32 GB 2 rank 2933

(End of data from sysinfo program)

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Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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SPECr temperature 2017 int base = 105
SPECr temperature 2017 int peak = 110

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Compiler Version Notes (Continued)

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C++ | 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---

C++ | 523.xalancbmk_r(peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---

Fortran | 548.exchange2_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
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(Test Sponsor: HPE)
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### Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

C benchmarks:
```
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

C++ benchmarks:
```
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:
```
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```
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**CPU2017 License:** 3  
**Test Sponsor:** HPE  
**Tested by:** HPE

### Peak Compiler Invocation

C benchmarks (except as noted below):  
`icc -m64 -std=c11`

$icc_r : gcc_r  
-32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):  
`icpc -m64`

$icpc_r : xalancbmk_r  
-m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:  
`ifort -m64`

### Peak Portability Flags

- **500.perlbench_r:** -DSPEC_LP64 -DSPEC_LINUX_X64  
- **502.gcc_r:** -D_FILE_OFFSET_BITS=64  
- **505.mcf_r:** -DSPEC_LP64  
- **520.omnetpp_r:** -DSPEC_LP64  
- **523.xalancbmk_r:** -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX  
- **525.x264_r:** -DSPEC_LP64  
- **531.deepsjeng_r:** -DSPEC_LP64  
- **541.leela_r:** -DSPEC_LP64  
- **548.exchange2_r:** -DSPEC_LP64  
- **557.xz_r:** -DSPEC_LP64

### Peak Optimization Flags

C benchmarks:  
- **500.perlbench_r:** -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

- **502.gcc_r:** -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-32/lib -ljemalloc

- **505.mcf_r:** -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10
(3.20 GHz, Intel Xeon Silver 4215R)

SPECrate®2017_int_base = 105
SPECrate®2017_int_peak = 110

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Peak Optimization Flags (Continued)

505.mcf_r (continued):
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leea_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml
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ProLiant DL380 Gen10  
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Test Date: Mar-2020  
Hardware Availability: Feb-2020  
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