Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base = 198</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak = 212</td>
</tr>
</tbody>
</table>

### Hardware
- **CPU Name:** Intel Xeon Gold 5218R
- **Max MHz:** 4000
- **Nominal:** 2100
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1, 2 chip(s)
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 27.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2666)
- **Storage:** 1 x 400 GB SAS SSD, RAID 0
- **Other:** None

### Software
- **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64) Kernel 4.12.14-195-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux;
- **Parallel:** No
- **Firmware:** HPE BIOS Version I42 v2.22 (11/13/2019) released Feb-2020
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

---

**SPEC CPU®2017 Floating Point Rate Result**

**Test Sponsor:** HPE

**Hewlett Packard Enterprise**

**Copyright 2017-2020 Standard Performance Evaluation Corporation**
### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>80</td>
<td>1725</td>
<td>465</td>
<td>1724</td>
<td>465</td>
<td>1726</td>
<td>465</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>80</td>
<td>586</td>
<td>173</td>
<td>588</td>
<td>172</td>
<td>587</td>
<td>173</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>80</td>
<td>501</td>
<td>152</td>
<td>499</td>
<td>152</td>
<td>495</td>
<td>154</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>80</td>
<td>1912</td>
<td>109</td>
<td>1911</td>
<td>110</td>
<td>1923</td>
<td>109</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>80</td>
<td>825</td>
<td>226</td>
<td>825</td>
<td>226</td>
<td>828</td>
<td>226</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>80</td>
<td>758</td>
<td>111</td>
<td>757</td>
<td>111</td>
<td>758</td>
<td>111</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>80</td>
<td>907</td>
<td>198</td>
<td>897</td>
<td>200</td>
<td>889</td>
<td>202</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>80</td>
<td>579</td>
<td>211</td>
<td>579</td>
<td>211</td>
<td>578</td>
<td>211</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>80</td>
<td>615</td>
<td>227</td>
<td>622</td>
<td>225</td>
<td>617</td>
<td>227</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>80</td>
<td>401</td>
<td>496</td>
<td>401</td>
<td>496</td>
<td>402</td>
<td>495</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>80</td>
<td>378</td>
<td>356</td>
<td>381</td>
<td>354</td>
<td>375</td>
<td>359</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>80</td>
<td>2031</td>
<td>153</td>
<td>2031</td>
<td>153</td>
<td>2026</td>
<td>154</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>80</td>
<td>1491</td>
<td>85.3</td>
<td>1488</td>
<td>85.5</td>
<td>1485</td>
<td>85.6</td>
</tr>
</tbody>
</table>

**SPECrate®2017_fp_base = 198**

**SPECrate®2017_fp_peak = 212**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
 sync; echo 3 > /proc/sys/vm/drop_caches
```

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.5

(Continued on next page)
General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
- Thermal Configuration set to Maximum Cooling
- Memory Patrol Scrubbing set to Disabled
- LLC Prefetch set to Enabled
- LLC Dead Line Allocation set to Disabled
- Enhanced Processor Performance set to Enabled
- Workload Profile set to General Throughput Compute
- Workload Profile set to Custom
- Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011
running on sy480-sys1 Tue Mar 10 15:35:58 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 20
  siblings : 40
  physical 0: cores 0 1 2 3 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 1: cores 0 1 2 3 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
  Architecture:          x86_64
  CPU op-mode(s):        32-bit, 64-bit
  Byte Order:            Little Endian
  Address sizes:         46 bits physical, 48 bits virtual
  CPU(s):                80
  On-line CPU(s) list:   0-79
  Thread(s) per core:    2

(Continued on next page)
## Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Core(s) per socket:</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Socket(s):</td>
<td>2</td>
</tr>
<tr>
<td>NUMA node(s):</td>
<td>4</td>
</tr>
<tr>
<td>Vendor ID:</td>
<td>GenuineIntel</td>
</tr>
<tr>
<td>CPU family:</td>
<td>6</td>
</tr>
<tr>
<td>Model:</td>
<td>85</td>
</tr>
<tr>
<td>Model name:</td>
<td>Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz</td>
</tr>
<tr>
<td>Stepping:</td>
<td>7</td>
</tr>
<tr>
<td>CPU MHz:</td>
<td>2100.000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>4200.00</td>
</tr>
<tr>
<td>Virtualization:</td>
<td>VT-x</td>
</tr>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>28160K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-9,40-49</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>10-19,50-59</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>20-29,60-69</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>30-39,70-79</td>
</tr>
<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmcgov mtrr stibp stibpd fsgsbase tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cmp xsaveopt xsaves cqm_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospk xsaveopt avx512_vnni md_clear flush_l1d arch_capabilities</td>
</tr>
</tbody>
</table>

/proc/cpuinfo cache data

**WARNING:** a numactl 'node' might or might not correspond to a physical chip.

### From numactl --hardware

<table>
<thead>
<tr>
<th>available: 4 nodes (0-3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>node 0 cpus: 0 1 2 3 4 5 6 7 8 9 40 41 42 43 44 45 46 47 48 49</td>
</tr>
<tr>
<td>node 0 size: 96286 MB</td>
</tr>
<tr>
<td>node 0 free: 95842 MB</td>
</tr>
<tr>
<td>node 1 cpus: 10 11 12 13 14 15 16 17 18 19 50 51 52 53 54 55 56 57 58 59</td>
</tr>
<tr>
<td>node 1 size: 96734 MB</td>
</tr>
<tr>
<td>node 1 free: 96476 MB</td>
</tr>
<tr>
<td>node 2 cpus: 20 21 22 23 24 25 26 27 28 29 60 61 62 63 64 65 66 67 68 69</td>
</tr>
<tr>
<td>node 2 size: 96764 MB</td>
</tr>
<tr>
<td>node 2 free: 96564 MB</td>
</tr>
</tbody>
</table>

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 212

Platform Notes (Continued)

node 3 cpus: 30 31 32 33 34 35 36 37 38 39 70 71 72 73 74 75 76 77 78 79
node 3 size: 96566 MB
node 3 free: 96366 MB
node distances:
node 0 1 2 3
0: 10 21 31 31
1: 21 10 31 31
2: 31 31 10 21
3: 31 31 21 10

From /proc/meminfo
MemTotal: 395624396 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux sy480-sys1 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 10 15:34

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 btrfs 371G 93G 277G 26% /home

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 212

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
  BIOS: HPE I42 11/13/2019
  Vendor: HPE
  Product: Synergy 480 Gen10
  Product Family: Synergy
  Serial: MXQ7380505

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
  24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

C
  519.lbm_r(base, peak) 538.imagick_r(base, peak)
  544.nab_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
  508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C
  511.povray_r(base, peak) 526.blender_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Hewlett Packard Enterprise (Test Sponsor: HPE)
Synergy 480 Gen10 (2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 212

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Compiler Version Notes (Continued)

C++, C, Fortran | 507.cactuBSSN_r(base, peak)
-----------------------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------------------------
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
  | 554.roms_r(base, peak)
-----------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
-----------------------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64
Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
SPEC CPU®2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 212

<table>
<thead>
<tr>
<th>CPU2017 License: 3</th>
<th>Test Date: Mar-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Feb-2020</td>
</tr>
<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Jun-2019</td>
</tr>
</tbody>
</table>

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
- qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
- align array32byte

Benchmarks using both C and C++:
- xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
- xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
- qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
- align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags
Hewlett Packard Enterprise
(Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 212

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Peak Optimization Flags

C benchmarks:

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

(Continued on next page)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrate®2017_fp_base = 198
SPECrate®2017_fp_peak = 212

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Peak Optimization Flags (Continued)

526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-10 15:35:57-0400.
Originally published on 2020-04-10.