Hewlett Packard Enterprise
(Spec Sponsor: HPE)
Synergy 480 Gen10
(3.40 GHz, Intel Xeon Gold 6246R)

SPEC®2017_int_base = 10.4
SPEC®2017_int_peak = 10.5

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Hardware
CPU Name: Intel Xeon Gold 6246R
Max MHz: 4100
Nominal: 3400
Enabled: 32 cores, 2 chips
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 35.75 MB I+D on chip per chip
Other: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 400 GB SAS SSD, RAID 0
Other: None

Software
OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)
Kernel 4.12.14-195-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++
Compiler Build 20190416 for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran
Compiler Build 20190416 for Linux;
Parallel: Yes
Firmware: HPE BIOS Version I42 v2.22 (11/13/2019) released Feb-2020
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
### SPEC CPU®2017 Integer Speed Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(3.40 GHz, Intel Xeon Gold 6246R)

**SPECspeed®2017_int_base = 10.4**  
**SPECspeed®2017_int_peak = 10.5**

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<td>6.83</td>
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<tr>
<td>605.mcf_s</td>
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<tr>
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<td>4.81</td>
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<tr>
<td>648.exchange2_s</td>
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<tr>
<td>657.xz_s</td>
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<td>266</td>
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<td>267</td>
<td>23.2</td>
<td>267</td>
<td>23.1</td>
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<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

#### Operating System Notes

- Stack size set to unlimited using "ulimit -s unlimited"
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```bash
  sync; echo 3 > /proc/sys/vm/drop_caches
  ```

#### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

#### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
- NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
## Platform Notes

### BIOS Configuration:
- Hyper-Threading set to Disabled
- Thermal Configuration set to Maximum Cooling
- Memory Patrol Scrubbing set to Disabled
- LLC Prefetch set to Enabled
- LLC Dead Line Allocation set to Disabled
- Enhanced Processor Performance set to Enabled
- Workload Profile set to General Peak Frequency Compute
- Energy/Performance Bias set to Balanced Power
- Workload Profile set to Custom
- Numa Group Size Optimization set to Flat
- Intel UPI Link Power Management set to Enabled

### Sysinfo program
```
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e646a485a0011
running on sy480-sys2 Sun Mar 1 02:36:06 2020
```

### SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

### From /proc/cpuinfo
```
model name : Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 1 2 3 9 12 13 16 17 18 19 22 26 27 28 29
physical 1: cores 0 1 2 3 5 6 9 11 12 16 18 19 20 26 28 29
```

### From lscpu:
```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
```

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes (Continued)

Stepping: 7
CPU MHz: 3400.000
BogoMIPS: 6800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-15
NUMA node1 CPU(s): 16-31
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_p impres mcm ssbd ibbs ibbp ibrs Enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mxp rdt a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xasvec xsavec xsavec cqm_llc cqm_occup_llc cqm_mbnum_total cqm_mbnum_local dtherm ida arat pln pts pkw ospke avx512_vnni md_clear flush_lld arch_capabilities

/proc/cpuinfo cache data

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 193025 MB
node 0 free: 192633 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 193336 MB
node 1 free: 192948 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 395634796 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:

(Continued on next page)
## SPEC CPU®2017 Integer Speed Result

### Hewlett Packard Enterprise

**Test Sponsor:** HPE  
**System:** Synergy 480 Gen10  
**Processor:** (3.40 GHz, Intel Xeon Gold 6246R)  
**CPU2017 License:** 3  
**Test Date:** Mar-2020  
**Hardware Availability:** Feb-2020  
**Test Sponsor:** HPE  
**Tested by:** HPE  
**Software Availability:** Jun-2019

### SPECspeed®2017 Int Base = 10.4
### SPECspeed®2017 Int Peak = 10.5

### Platform Notes (Continued)

```plaintext
NAME="SLES"  
VERSION="15-SP1"  
VERSION_ID="15.1"  
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
   Linux sy480-sys2 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 1 02:34

SPEC is set to: /home/cpu2017
   Filesystem     Type   Size  Used Avail Use% Mounted on
   /dev/sda2      btrfs  371G   27G  343G   8% /home

From /sys/devices/virtual/dmi/id
   BIOS:       HPE I42 11/13/2019
   Vendor:     HPE
   Product:    Synergy 480 Gen10
   Product Family: Synergy
   Serial:     MXQ7380505

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
   24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

(End of data from sysinfo program)
```
SPEC CPU®2017 Integer Speed Result

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Compiler Version Notes

<table>
<thead>
<tr>
<th>Language</th>
<th>Base Benchmark (Base, Peak)</th>
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<tbody>
<tr>
<td>C</td>
<td>600.perlbench_s (base, peak), 602.gcc_s (base, peak), 605.mcf_s (base, peak), 625.x264_s (base, peak), 657.xz_s (base, peak)</td>
</tr>
</tbody>
</table>

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

<table>
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<tr>
<th>Language</th>
<th>Base Benchmark (Base, Peak)</th>
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<tbody>
<tr>
<td>C++</td>
<td>620.omnetpp_s (base, peak), 623.xalancbmk_s (base, peak), 631.deepsjeng_s (base, peak), 641.leela_s (base, peak)</td>
</tr>
</tbody>
</table>

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

<table>
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<tr>
<th>Language</th>
<th>Base Benchmark (Base, Peak)</th>
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<tbody>
<tr>
<td>Fortran</td>
<td>648.exchange2_s (base, peak)</td>
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</tbody>
</table>

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
```

(Continued on next page)
Hewlett Packard Enterprise  
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**SPEC CPU®2017 Integer Speed Result**  
Copyright 2017-2020 Standard Performance Evaluation Corporation  

<table>
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<td>SPECspeed®2017_int_peak</td>
<td>10.5</td>
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</tbody>
</table>

**Base Portability Flags (Continued)**

623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX  
625.x264_s: -DSPEC_LP64  
631.deepsjeng_s: -DSPEC_LP64  
641.leela_s: -DSPEC_LP64  
648.exchange2_s: -DSPEC_LP64  
657.xz_s: -DSPEC_LP64  

**Base Optimization Flags**

C benchmarks:  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/usr/local/je5.0.1-64/lib -ljemalloc  

C++ benchmarks:  
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64  
-lqkmalloc  

Fortran benchmarks:  
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs  

**Peak Compiler Invocation**

C benchmarks:  
icc -m64 -std=c11  

C++ benchmarks:  
icpc -m64  

Fortran benchmarks:  
ifort -m64  

**Peak Portability Flags**

Same as Base Portability Flags
Hewlett Packard Enterprise  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(3.40 GHz, Intel Xeon Gold 6246R)  

SPEC 2017 Integer Speed Result  

Copyright 2017-2020 Standard Performance Evaluation Corporation  

SPECspeed®2017_int_base = 10.4  

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CPU2017 License: 3  
Test Sponsor: HPE  
Tested by: HPE  

Test Date: Mar-2020  
Hardware Availability: Feb-2020  
Software Availability: Jun-2019  

Peak Optimization Flags  

C benchmarks:  

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -CORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:  

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -CORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:  

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
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Test Date: Mar-2020  
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Peak Optimization Flags (Continued)  
Fortran benchmarks (continued):  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html  

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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