## SPEC CPU®2017 Integer Speed Result

### Cisco Systems

**Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)**

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>Cisco Systems</th>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Mar-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Feb-2020</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thread</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>16</td>
<td>6.51</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>16</td>
<td>8.72</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>16</td>
<td>5.26</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>16</td>
<td>3.17</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>16</td>
<td>13.5</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>16</td>
<td>4.90</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>16</td>
<td>4.90</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>657.xz_s</td>
<td>16</td>
<td></td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Silver 4215R  
  - Max MHz: 4000  
  - Nominal: 3200  
  - Enabled: 16 cores, 2 chips  
  - Orderable: 1.2 Chips  
  - Cache L1: 32 KB I + 32 KB D on chip per core  
  - L2: 1 MB I+D on chip per core  
  - L3: 11 MB I+D on chip per chip  
  - Other: None  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
- **Storage:** 1 x 240 GB SSD SATA  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  - 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.4i released Aug-2019  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perbench_s</td>
<td>16</td>
<td>274</td>
<td>6.48</td>
<td>273</td>
<td>6.51</td>
<td>273</td>
<td>6.51</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>16</td>
<td>459</td>
<td>8.67</td>
<td>456</td>
<td>8.74</td>
<td>457</td>
<td>8.72</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>16</td>
<td>383</td>
<td>12.3</td>
<td>385</td>
<td>12.3</td>
<td>384</td>
<td>12.3</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>16</td>
<td>310</td>
<td>5.26</td>
<td>311</td>
<td>5.24</td>
<td>309</td>
<td>5.27</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>16</td>
<td>115</td>
<td>12.3</td>
<td>116</td>
<td>12.2</td>
<td>115</td>
<td>12.4</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>16</td>
<td>131</td>
<td>13.4</td>
<td>131</td>
<td>13.5</td>
<td>131</td>
<td>13.5</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>16</td>
<td>260</td>
<td>5.51</td>
<td>260</td>
<td>5.51</td>
<td>260</td>
<td>5.51</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>16</td>
<td>349</td>
<td>4.89</td>
<td>348</td>
<td>4.90</td>
<td>348</td>
<td>4.90</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>16</td>
<td>173</td>
<td>17.0</td>
<td>172</td>
<td>17.1</td>
<td>171</td>
<td>17.1</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>16</td>
<td>316</td>
<td>19.6</td>
<td>316</td>
<td>19.6</td>
<td>316</td>
<td>19.6</td>
</tr>
</tbody>
</table>

SPECspeed®2017_int_base = 9.42
SPECspeed®2017_int_peak = 9.59

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the Redhat Enterprise 7.5, and the system compiler gcc 4.8.5
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_int_base = 9.42
SPECspeed®2017_int_peak = 9.59

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Mar-2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Feb-2020</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
running on linux-cud8 Sun Mar 8 22:14:39 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
2 "physical id"s (chips)
16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
Stepping: 7
CPU MHz: 3200.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 6400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>9.42</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>9.59</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdpc_13 invpcid_single intel_pni mba tpr_shadow vmvi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rdvi rtm cqm mpx rd tỤ avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsavesopt xsaveopt xsave xsetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pni pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/platform_cache_size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 385636 MB
  node 0 free: 385022 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 387029 MB
  node 1 free: 386999 MB
  node distances:
    node  0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 791209624 KB
  MemFree: 15025007 MB
  MemAvailable: 540959557 KB
  TotalSwap: 0 KB
  FreeSwap: 0 KB
  SwapTotal: 0 KB
  SwapFree: 0 KB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"

  (Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Specspeed®2017_int_base = 9.42
Specspeed®2017_int_peak = 9.59

Platform Notes (Continued)

```bash
ANSI_COLOR="0;32" CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
    via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted
    Speculation, IBPB, IBRS_FW

run-level 3 Mar 8 22:08
SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda2 btrfs 224G 38G 185G 18% /home

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. C220M5.4.0.41.0.0831191119 08/31/2019
    Vendor: Cisco Systems Inc
    Product: UCSC-C220-M5SX
    Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)
```

Compiler Version Notes

```
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base,
    | peak) 625.x264_s(base, peak) 657.xz_s(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)
## Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 9.42</th>
<th>SPECspeed®2017_int_peak = 9.59</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
<td>Test Date: Mar-2020</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Feb-2020</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

### Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```
==============================================================================
C++       | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak)
          | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
==============================================================================
Fortran    | 648.exchange2_s(base, peak)
-----------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

### Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

### Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_int_base = 9.42
SPECspeed®2017_int_peak = 9.59

CPU2017 License: 9019  Test Date:            Mar-2020
Test Sponsor:  Cisco Systems    Hardware Availability: Feb-2020
Tested by:  Cisco Systems     Software Availability: May-2019

Base Portability Flags (Continued)

657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
- L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
- Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
- lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
- nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Peak Portability Flags

Same as Base Portability Flags
### SPEC CPU®2017 Integer Speed Result

**Cisco Systems**
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)  

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>9.42</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>9.59</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Mar-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

---

#### Peak Optimization Flags

**C benchmarks:**

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

**Fortran benchmarks:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

---

*(Continued on next page)*
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECspeed®2017_int_base = 9.42
SPECspeed®2017_int_peak = 9.59

Peak Optimization Flags (Continued)

Fortran benchmarks (continued):
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

Originally published on 2020-04-17.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

Tested with SPEC CPU®2017 v1.1.0 on 2020-03-09 01:14:39-0400.
Originally published on 2020-04-17.