# SPEC CPU®2017 Floating Point Rate Result

## Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4215R, 3.20GHz)

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## Hardware
- **CPU Name:** Intel Xeon Silver 4215R
- **Max MHz:** 4000
- **Nominal:** 3200
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 960 GB SSD SAS
- **Other:** None

## Software
- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4215R, 3.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Results Table

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SPECrate®2017_fp_base = 93.5
SPECrate®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using **ulimit -s unlimited**

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
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Cisco UCS B200 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECrater®2017_fp_base = 93.5
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CPU2017 License: 9019
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General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
running on linux-13s9 Sat Mar 14 18:12:21 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
 2  "physical id"s (chips)
 32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2

(Continued on next page)
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Tested by: Cisco Systems

Hardware Availability: Feb-2020
Software Availability: May-2019

Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
Stepping:            7
CPU MHz:             3200.000
CPU max MHz:         4000.0000
CPU min MHz:         1000.0000
BogoMIPS:            6400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            11264K
NUMA node0 CPU(s):   0-7,16-23
NUMA node1 CPU(s):   8-15,24-31
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbe fma cx16 xtrr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pppin mba tpr_shadow vmlinux flexpriority ept
vpid fsgrbase tsc_adjust bni hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 16 17 18 19 20 21 22 23
node 0 size: 386532 MB
node 0 free: 380335 MB
node 1 cpus: 8 9 10 11 12 13 14 15 24 25 26 27 28 29 30 31
node 1 size: 387045 MB
node 1 free: 382570 MB
node distances:
  node  0  1
  0: 10  21
  1: 21  10

From /proc/meminfo
MemTotal: 792144224 KB

(Continued on next page)
Platform Notes (Continued)

HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
    os-release:
      NAME="SLES"
      VERSION="15"
      VERSION_ID="15"
      PRETTY_NAME="SUSE Linux Enterprise Server 15"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-13s9 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 14:14

SPEC is set to: /home/cpu2017
  Filesystem  Type  Size  Used Avail Use% Mounted on
  /dev/sdb6  xfs  755G  17G  738G  3%  /home

From /sys/devices/virtual/dmi/id
  BIOS:  Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Vendor:  Cisco Systems Inc
  Product:  UCSB-B200-M5
  Serial:  FCH21437KVH

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

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Cisco Systems
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<tr>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

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<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4215R, 3.20GHz)

SPECrated2017_fp_base = 93.5
SPECrated2017_fp_peak = Not Run

Compiler Version Notes (Continued)

Fortran  |  503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
---------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---------------------------------------------------------------------

Fortran, C  |  521.wrf_r(base) 527.cam4_r(base)
---------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64

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## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Silver 4215R, 3.20GHz)

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### Base Portability Flags (Continued)

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- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**C++ benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**Fortran benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

**Benchmarks using both C and C++:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
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The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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