# SPEC CPU®2017 Integer Rate Result

**Cisco Systems**
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>218</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak</td>
<td>228</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019
**Test Date:** Mar-2020

**Test Sponsor:** Cisco Systems
**Hardware Availability:** Feb-2020

**Tested by:** Cisco Systems
**Software Availability:** May-2019

## Copies

<table>
<thead>
<tr>
<th>Benchmark</th>
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</tr>
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<tbody>
<tr>
<td>perlbench_r</td>
<td>80</td>
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<tr>
<td>gcc_r</td>
<td>80</td>
</tr>
<tr>
<td>mcf_r</td>
<td>80</td>
</tr>
<tr>
<td>omnetpp_r</td>
<td>80</td>
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<td>xalancbmk_r</td>
<td>80</td>
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<td>x264_r</td>
<td>80</td>
</tr>
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<td>80</td>
</tr>
<tr>
<td>leela_r</td>
<td>80</td>
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<tr>
<td>exchange2_r</td>
<td>80</td>
</tr>
<tr>
<td>xz_r</td>
<td>80</td>
</tr>
</tbody>
</table>

**SPECrate®2017_int_base (218)**
**SPECrate®2017_int_peak (228)**

## Hardware

**CPU Name:** Intel Xeon Gold 5218R
**Max MHz:** 4000
**Nominal:** 2100
**Enabled:** 40 cores, 2 chips, 2 threads/core
**Orderable:** 1.2 Chips
**Cache L1:** 32 KB I + 32 KB D on chip per core
**Cache L2:** 1 MB I+D on chip per core
**Cache L3:** 27.5 MB I+D on chip per chip
**Other:** None
**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
**Storage:** 1 x 240 GB SSD SATA
**Other:** None

## Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64)
**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
**Fortran:** Version 19.0.4.227 of Intel Fortran Compiler for Linux
**Parallel:** No
**Firmware:** Version 4.0.4b released Apr-2019
**File System:** btrfs
**System State:** Run level 3 (multi-user)
**Base Pointers:** 64-bit
**Peak Pointers:** 32/64-bit
**Other:** jemalloc memory allocator V5.0.1
**Power Management:** BIOS set to prefer performance at the cost of additional power usage
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### Cisco Systems

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<table>
<thead>
<tr>
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<td>512</td>
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<td>512</td>
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<td>597</td>
<td>145</td>
<td>596</td>
<td>145</td>
<td>596</td>
</tr>
</tbody>
</table>

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9–7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

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SPECraten®2017_int_base = 218
SPECraten®2017_int_peak = 228

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1e6e46a485a0011

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per core: 20

(Continued on next page)
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Platform Notes (Continued)

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2100.000
CPU max MHz: 4000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags:

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

/cache data
   cache size : 28160 KB

https://www.spec.org/
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### Platform Notes (Continued)

- **node 2 free:** 193274 MB  
- **node 3 cpus:** 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79  
- **node 3 size:** 193490 MB  
- **node 3 free:** 193239 MB  
- **node distances:**  
  - 0: 10 11 21 21  
  - 1: 11 10 21 21  
  - 2: 21 21 10 11  
  - 3: 21 21 11 10  

From `/proc/meminfo`  
- `MemTotal:` 791167672 kB  
- `HugePages_Total:` 0  
- `Hugepagesize:` 2048 kB  

From `/etc/*release* /etc/*version*`  
- `NAME="SLES"`  
- `VERSION="15"`  
- `VERSION_ID="15"`  
- `PRETTY_NAME="SUSE Linux Enterprise Server 15"`  
- `ID="sles"`  
- `ID_LIKE="suse"`  
- `ANSI_COLOR="0;32"`  
- `CPE_NAME="cpe:/o:suse:sles:15"`  

**uname -a:**  
```
Linux linux-bo6o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

**Kernel self-reported vulnerability status:**  
- **CVE-2018-3620 (L1 Terminal Fault):** No status reported  
- **Microarchitectural Data Sampling:** No status reported  
- **CVE-2017-5754 (Meltdown):** Not affected  
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via `prctl` and `seccomp`  
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization  
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW  

**run-level 3 Mar 14 13:25**  

**SPEC is set to:** `/home/cpu2017`  

<table>
<thead>
<tr>
<th align="center">Filesystem</th>
<th align="center">Type</th>
<th align="center">Size</th>
<th align="center">Used</th>
<th align="center">Avail</th>
<th align="center">Use%</th>
<th align="center">Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td align="center">/dev/sdb1</td>
<td align="center">btrfs</td>
<td align="center">224G</td>
<td align="center">6.6G</td>
<td align="center">217G</td>
<td align="center">3%</td>
<td align="center">/home</td>
</tr>
</tbody>
</table>

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Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Vendor: Cisco Systems Inc
Product: UCSB-B200-M5
Serial: FCH21437LAT

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C       | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++  | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++  | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
      531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++  | 523.xalancbmk_r(peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++  | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
      531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
## Base Compiler Invocation

C benchmarks:
```bash
icc -m64 -std=c11
```

C++ benchmarks:
```bash
icpc -m64
```

Fortran benchmarks:
```bash
ifort -m64
```

## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
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<td>-DSPEC_LP64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>-DSPEC_LP64</td>
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<td>531.deepsjeng_r</td>
<td>-DSPEC_LP64</td>
</tr>
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<td>548.exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

### C benchmarks:
```bash
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

### C++ benchmarks:
```bash
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

### Fortran benchmarks:
```bash
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```
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Peak Compiler Invocation
C benchmarks (except as noted below):
icc -m64 -std=c11


C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r:icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags
C benchmarks:
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lgkmalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4

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Peak Optimization Flags (Continued)

505.mcf_r (continued):
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

525.x264_r -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -fno-alias
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

523.xalancbmk_r -W1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
- xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
- L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:

-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
  -lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
## SPEC CPU®2017 Integer Rate Result

### Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>218</th>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  

**Test Date:** Mar-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

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