Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrater®2017_fp_base = 66.3
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Bronze 3206R
Max MHz: 1900
Nominal: 1900
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)
Storage: 1 x 240 GB SSD SATA
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage
# SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

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**Results Table**

**SPECrate®2017_fp_base = 66.3**

**SPECrate®2017_fp_peak = Not Run**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrate®2017_fp_base = 66.3
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Mar-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
running on linux-us1o Sat Mar 14 21:38:53 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
  siblings : 8
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrater®2017_fp_base = 66.3
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Vendor ID:       GenuineIntel
CPU family:     6
Model:          85
Model name:     Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
Stepping:       7
CPU MHz:        1900.000
CPU max MHz:    1900.0000
CPU min MHz:    1000.0000
BogoMIPS:       3800.00
Virtualization: VT-x
L1d cache:      32K
L1i cache:      32K
L2 cache:       1024K
L3 cache:       11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15
Flags:          fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
                sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
                epb cat_l3 cdp_l3 invpcid_single intel_pippin mba flexpriority ept
                vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  invpcid rtm cqm mpx rdt_a
                avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
                xsaveopt xsave xcrpt xsavec xgetbv1 xsaves cqm_llc cqm_occu_llc cqm_mbm_total
                cqm_mbm_local ibpb ibrs stibp dtherm arat pni pln pts hwp hwp_act_window
                hwp_epp hwp_prgm_req pkup ospe
                avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
  cache size : 11264 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7
  node 0 size: 386374 MB
  node 0 free: 381195 MB
  node 1 cpus: 8 9 10 11 12 13 14 15
  node 1 size: 387047 MB
  node 1 free: 384063 MB
  node distances:
  node  0 1
  0:  10 21
  1:  21 10

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrate®2017_fp_base = 66.3
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

MemTotal: 791984136 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-us1o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
    via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 17:29

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sdb2 btrfs 224G 13G 211G 6% /home

From /sys/devices/virtual/dmi/id
    BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
    Vendor: Cisco Systems Inc
    Product: UCSB-B200-M5
    Serial: FCH22137XAV

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrate®2017_fp_base = 66.3
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Test Date: Mar-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133

(End of data from sysinfo program)

Compiler Version Notes

C

| 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++

| 508.namd_r(base) 510.parest_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C

| 511.povray_r(base) 526.blender_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran

| 507.cactuBSSN_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
### Compiler Version Notes (Continued)

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### Base Compiler Invocation

**C benchmarks:**
```bash
icc -m64 -std=c11
```

**C++ benchmarks:**
```bash
icpc -m64
```

**Fortran benchmarks:**
```bash
ifort -m64
```

**Benchmarks using both Fortran and C:**
```bash
ifort -m64 icc -m64 -std=c11
```

**Benchmarks using both C and C++:**
```bash
icpc -m64 icc -m64 -std=c11
```

**Benchmarks using Fortran, C, and C++:**
```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

### Base Portability Flags

503.bwaves_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
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Hardware Availability: Feb-2020
Software Availability: May-2019

Base Portability Flags (Continued)

507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

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The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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